**Motivation**

- H.264/AVC is nowadays the de-facto standard for video applications, due to its high coding efficiency and flexibility.
- The computational complexity of the video coding algorithms in H.264/AVC significantly limits its usage in SoCs of low and medium complexity.
- Modern multimedia SoCs consist of quite complex heterogeneous multi-core structures with one GPP and multiple specialized processing cores, in order to speedup the execution of the most complex and time consuming operations.
- Efficient hardware / software co-design strategies must therefore be employed so that the required system performance levels can be achieved.
- Tight area / power / performance constraints demand customized implementations, which significantly increase the cost and the development time of such SoCs.

**Multi-Core Video Encoder**

**Step 1**
- The hardware component is based on the GRLIB platform;
- A Leon3 soft-core was used to implement the system CPU;
- An improved version of an ASPIC IP core [2] was used to realize the ME operation;
- Interconnections are based on the AMBA AHB and APB buses.

**Step 2**
- The APB ME processor user programming interface consists of 3 sets of memory mapped registers;
- Four 32-bit registers allow to control and evaluate the core operation;
- Three 32-bit registers allow to upload the firmware to the core program RAM and the pixel data to the core data RAMs;
- Three 32-bit registers allow to retrieve the results of the ME operation.

**Step 3**
- The hardware wrapper adapts the ASPIC interface to the AMBA APB interface;
- Implements the proposed user programming interface;
- Supports run-time debug facility of the ASPIC operation;
- Allows the ASPIC, Leon3 and AMBA interfaces to operate with different clock frequencies.

**Step 4**
- Fine tuning of the p264 [1] platform to optimize the interaction between the software application and the ME core;
- A simple and effective API supports the user programming interface of the ME core;
- The data transfer operations occur in parallel with the estimation of MVs.

**H.264/AVC Framework**

- Can be used to develop generic multi-core SoCs for H.264/AVC video encoding;
- Based on an efficient hardware / software co-design approach;
- Both the hardware and the software components are highly modular and flexible architectures that do not depend on each other.

**Software Component**
- Software program implementing the video encoding application;
- It consists of an adapted version of the p264 programming platform [1] targeting efficient SoC implementations;
- p264 is fully compliant with the H.264/AVC reference software (JM14).

**Hardware Component**
- Addresses the hardware implementation issues regarding the integration of new cores in the multi-core SoC structure;
- Implements a methodology that allows to significantly reduce the design time;
- Guarantees minimum losses in system performance due to core integration issues.

**Implementation Results**

- The multi-core architecture was implemented in a GR-GPCI-XC4V development board, which includes a Xilinx Virtex4 FPGA;
- Low hardware requirements for the multi-core H.264/AVC video encoder SoC;
- About 3% of the hardware resources are used to implement the APB interface of the ME IP core;
- It is possible to compute MVs for QCIF video sequences is real-time.

**Performance Results**

- Huge reduction in the computation time of the ME operation;
- Transfer times corresponding to the pixel data (MB and SA) and the ME results (MVs) are negligible: about 0.1% of the total encoding time;
- The obtained speedup values and communication times successfully validate the proposed framework.

**Most relevant publications:**


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Tiago Dias
Tiago.Dias@inesc-id.pt