A Microelectrode Stimulation System for a Cortical Neuroprosthesis

AD/DA System

Miguel Santos, Miguel Martins, Jorge Fernandes, Moisés Piedade

Project FCT: PTDC/EEA-ELC/68972/2006

November 2008
September 2010
Report Goal
This internal report intends to describe the present development state of the integrated microelectrode stimulator for the intracortical neuroprosthesis. Note that this report has evolved from the paper “A Microelectrode Stimulation System for a Cortical Neuroprosthesis” accepted in the Conference on Design of Circuits and Integrated Circuits, DCIS’06, realized in 2006. The main goals of this report are:

• a description of the complete project (section II);
• a description of the system architecture (section III);
• a description of the circuit proposal for the microelectrode stimulation system (section IV);
• an introduction to the new project challenges (section V);
• an evaluation of the future work (section VI).

1. DESCRIPTION OF THE SYSTEM

Biomedical applications have seen an intense research effort in the last few years. Due to its huge complexity it is a multidisciplinary area where microelectronics plays an important role for the feasibility of most systems. Implantable stimulators for biomedical applications, most commonly applied, are in the area of muscular or nerve stimulation, for heart, limbs or hearing diseases [1-3]. Some of these applications, such as pacemakers, require very low power systems, to avoid the replacement of batteries, but its action requires also almost no signal processing.

Biomedical implementations in the field of visual rehabilitation, is in its early stages. Besides the mechanical and optic mechanisms associated with vision which are already fully understood and can be corrected by surgery or external lenses, other mechanisms like the image processing that takes place from the retina down to the visual cortex is still not well known.

Recently research results on experiments to stimulate the visual cortex to improve the quality of life for blind or partially blind people have been presented [4-7]. In this paper we address an integrated microelectrode stimulator for intracortical neuroprosthesis. The system architecture was presented in [8] where the system is divided in two parts: a primary system placed outside the human body where all the processing takes place, and a secondary system, placed inside the human head, just to activate the electrode array implanted in the visual cortex (Figure 1).
The first solutions to interface the implant with data and power were by a wired link [4]. However, it requires a large number of wires and, apart from the discomfort; it poses a high risk of infection. With RF coupling, data and power can be obtained directly from an RF low-coupling transformer discarding the need for batteries or wiring.

Here, we address the implantable microelectrode stimulator which uses flip-chip technology to be fully implantable without wiring, reducing the risk of infection and increasing robustness. It is small enough to be undetectable and requires a power on the order of miliwatts which can be obtained from the low power RF carrier itself.

II. SYSTEM ARCHITECTURE

The system architecture represented in Figure 2 [8] has two parts connected by an RF link: a primary system responsible for the processing which is placed outside the human body, and a secondary system, placed inside the human head, which obtains energy from the signal through the RF link and recovers the data and the clock.
The system has two RF links in the same transformer: the forward link where a power/data signal is transmitted using Frequency Shift Keying (FSK) modulation with a 10 MHz frequency carrier and up to 1 Mbps data bit rate and a backward link where data is transmitted in the reverse direction using DBPSK modulation with a 1.25 MHz frequency carrier data bit rate is up to 156.25 kbps. The secondary power, data and main system clock are derived from the forward link signal. After demodulation and frame disassembly, useful data is forwarded to the electrode stimulator. After demodulation and frame disassembly, useful data is forwarded to the electrode stimulator. This paper addresses the “control unit and electrode stimulator” block, and the “electrode sensing” block (Figure 2) as these are the most sensitive analog circuits of the system. A prototype with 4 electrode stimulators is being layout in a VLSI CMOS technology (0.35µm).

III. IMPLANTABLE SOLUTION PROPOSED

A. Microelectrodes Description

The circuit described in this project is to be implemented in an array of microelectrodes, which is a matrix of 10 by 10 and has a total area of 4.2x4.2mm². The number of electrodes in a microelectrode array is limited due to technology issues; the size of each electrode is limited by mechanical robustness and the enlargement of the matrix is ineffective because the brain is not plain, and there is an ideal deepness in the visual cortex that should be stimulated. Therefore, with the available technology it is just possible to implant several arrays.
The Electrode Stimulator block is responsible for stimulating the electrodes and is essentially a digital-to-analog converter (DAC). The Control Unit block is a digital controller that provides the Electrode Stimulator with the current amplitude and the duration of stimulation in clock cycles. It also controls the charge/discharge mode of the DAC.

The two most opposite solutions are to have: only one DAC with the output addressed to the chosen electrode, or a DAC for each electrode. We have favoured the second, because it gives more flexibility, we can address several electrodes at the same time, and if any problem should occur in one electrode, all the other can keep on functioning.

The problem of such solution would appear to be power and area, but we solve the area problem because we decided to do a flip-chip circuit to be placed directly in the microelectrode array (represented in Figure 3). This, removes the need for wiring, reduces overall size and increases reliability. Therefore, each Control Unit and Electrode Stimulator blocks are located at the base of a microelectrode, the circuit with the DAC and the digital controller can occupy an area equal to a microelectrode, which has 0.42x0.42mm$^2$, not to waste die area.

Regarding power, although the circuit is to be powered externally, special care has to be taken to reduce the power consumption. The available energy extracted from the input (modulated) signal is low, because the signal is sent through a transformer with a low $k$ factor [8]. The power issue is overcome having each DAC in idle mode and being only activated when the respective electrode is addressed.

Figure 3: Flip-chip solution for the electrode matrix and electrode stimulator circuit.
Special care has to be taken not to harm the patient with an accumulation of electric charges in his brain. The microelectrode has to be discharged after being charged and both phases have to have similar behaviour.

The DAC has to stimulate a microelectrode for $2T$ seconds with a maximum current $I$. Such stimulation consists in charging the load with a pre-determined current amplitude $I$ for $T$ seconds and, after that, discharging the microelectrode with the same current amplitude $I$ for $T$ seconds. It also has to support an output voltage variation of $\pm 1\text{V}$. The microelectrode is represented by a $10\text{k}\Omega$ resistance and a $2\text{pF}$ capacitance and is connected to ground. The stimulation has a maximum of $T=100\text{\mu s}$ and $I=100\text{\mu A}$. The duration and the amplitude of the stimulation are controlled by two five bits signals. The expected output of the Electrode Stimulator is represented in Figure 4.

One main issue considering this application is that the impedance of the electrode changes for each patient and even for each electrode. It is therefore, necessary to monitor what is happening in each electrode when addressed in a system calibration mode after the system is implanted. This makes necessary a backward link where an ADC is used to sense the voltage at the electrode. This ADC is shared by all the electrodes and in test mode only one electrode should be addressed at a time.

![Figure 4: Charge/discharge cycle of a stimulated electrode.](image)

### b. Circuits Description

All the circuits presented here were designed and simulated for process and mismatch variations. Power supply voltage variations are compensated by a self compensated bias circuit with a start-up circuitry, tolerant for such variations. The temperature was set to 37º Celsius as this is the human body.
temperature. The power supply voltage is 3.3 V, with $V_{DD}=+1.65V$ and $V_{SS}=-1.65V$. The technology is a 0.35µm CMOS technology.

c. Electrode Stimulator (DAC)

The most important block to be designed is the DAC circuit. Although, the specifications in terms of frequency and resolution are not difficult to meet, other issues like ensuring equal charge and discharge of the brain for each electrode activity, settling time of the DAC when addressed and reduction of spikes in the transitions made the design more challenging.

![Electrode Stimulator](image)

**Figure 5: Electrode stimulator output stage (electrode buffer).**

The electrode buffer topology is represented in Figure 5. The topology has a current source connected to $V_{DD}$ which represents the five bit converter's output current. In phase $\phi_1$ and with switch $S_1$ on, the current from the converter is mirrored and is fed into the microelectrode. This is the charge phase. In phase $\phi_2$, with switch $S_1$ on, the current flows from the load through the converter. This is the discharge phase. This architecture does not ensure a similar behaviour between charging and discharging operations due to the use of a current mirror. Hence, mismatches between charge and discharge current should be prevented. Notice that the operation of charging the load is no different from discharging it, which ensures a good circuit performance, since the load seen by the converter is always the same. The circuit implementation using a wide swing cascode is represented in Figure 6.
The glitch in the microelectrode occurs when switch $S_1$ commutes. When the Electrode Stimulator block is enabled, in the transition from phase $\Phi_2$ to phase $\Phi_1$, while switch $S_1$ is off, the voltage at node $X$ (Figure 6) is almost 1.5V, and all switches have low resistance, working on the triode region because of the headroom available. When switch $S_1$ turns on, there will be a small resistance connecting two nodes with different voltages. Since node $X$ has a voltage of almost 1.5V and the output is grounded, the current spike can be significant. To prevent this glitch to occur, an extra switch (with a higher resistance) is placed in parallel ($S_{1a}$ and $S_{1b}$) lowering effectively the current spike.

In figure 7 is represented the complete DAC circuit, including the microelectrode stimulator, the control signals generator and the biasing circuit. The microelectrode stimulator circuit, the control signals generator circuit and the biasing circuit are represented respectively in figures 8, 9 and 10.
Figure 7: Complete DAC cadence schematic, including biasing and control signals.

Figure 8: Electrode Stimulator (DAC) cadence schematic.
D. Control Unit

The Control Unit block activates or configures the Electrode Stimulator block. The digital controller must allow the configuration of both the amplitude of the Electrode Stimulator's output current and the
duration of the stimulations that will be applied to the microelectrode, which is done by means of a counter respective to the clock master. It must also allow the Output Data Processing block to read such configurations. Hence, the digital controller has activated, read and write operations. The digital blocks are written in synthesizable Verilog to be incorporated with the DAC in each electrode slot. The digital block high level diagram is represented in Figure 11.

![Figure 11: Control unit digital fluxogram for each electrode stimulator.](image)

### E. Analog-to-Digital Converter

The ADC to be used in the backward link should have high impedance, low capacitance input in order not to disturb the electrode being measured. The required resolution for the ADC is 5 bits. A flash ADC was choose because it does not need extra signal clocks besides the reference clock and the number of bits is reduced leading to a tolerable number of comparators. In figure 12 is presented the complete ADC cadence schematic. Figure 13 represents the comparator array and the reference circuit and finally figure 14 represents the comparator circuit.

![Figure 12: Complete ADC cadence schematic, including biasing and control signals.](image)
Figure 13: Comparator array and reference generator cadence schematics.

Figure 14: Comparator schematic.
IV. SIMULATION RESULTS

Figure 15 represents the simulation result of the charge/discharge cycle of a stimulated electrode, where it can be observed that the spike is indeed negligible.

Figure 16 represents the ADC simulation results.

Figure 16: ADC simulation result.
v. FUTURE WORK

In this section we try to enumerate some future work that is planned. First of all, it is important to refer some differences on the present project that imply the circuit design. One major difference concerns the initial array of microelectrodes that was replaced by a comb of microelectrodes that will be produced at INESC-MN. This modification gives more freedom on the circuit die size specification, which was prior limited to the area occupied by a single microelectrode, i.e., 0.42x0.42mm². The present version allows the placement of the circuit die in one of the sides of the comb, which allows the possibility of using either normal bonding or flip-chip. This last advantage is beneficial in terms of cost and feasibility. Another difference consists in the way the microelectrode is built. In what is concerned with the microelectrode stimulators, the load impedance imposed by them is now purely capacitive instead of the previous resistive impedance. A synthesis of the future work is now itemized:

- re-simulation of the DAC circuit for a purely capacitive load;
- comparison of the advantages and disadvantages of using a SAR ADC instead of a Flash ADC, for a further study of the possibility of using a SAR ADC instead of the present Flash ADC;
- simulation of all circuits with Monte Carlo to evaluate the sensitivity of these circuits to technology variations;
- prototyping of the complete circuit in accordance with new specifications.

References


Contents
1 Introduction .......................................................................................................................... 19
  1.1 ADC Performance .......................................................................................................... 19
  1.2 Layout of the ADC ......................................................................................................... 20
    1.2.1 Layout details ............................................................................................................ 25
  1.3 Layout of the DAC ......................................................................................................... 26
    1.3.1 Layout details ............................................................................................................ 30
2 References: ...................................................................................................................... Error! Bookmark not defined.
INTRODUCTION

The aim of this report is to present some work and conclusions obtained during the layout of one DAC and ADC.

**ADC Performance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>5 bits</td>
</tr>
</tbody>
</table>
Layout of the ADC
Figure 1: ADC layout with pads.

Figure 2: ADC layout.
Figure 3: Comparator.

Figure 4: Comparator test.
Figure 5: Comparator test.
Figure 6: ADC pos-layout simulation.
**Layout details**

Figure 7. – Detail of the bottom of the ADC layout: bottom of the resistive ladder, descodification of comparators 28 to 31 and output buffers (to pads).

Figure 8. – Detail of the top of the ADC layout: delay generator, enable, top of the resistive ladder, descodification of comparator 0.
Figure 1: DAC layout with pads.
Figure 2: DAC layout.
Figure 4: DAC pos-layout test.
Figure 6: ADC pos-layout simulation.

Transient Response

- \( V_{in} \)
- \( \text{bit}<0> \)
- \( \text{bit}<1> \)
- \( \text{bit}<2> \)
- \( \text{bit}<3> \)
- \( \text{bit}<4> \)

\( \text{clock} \)

Time (s)
Figure 7. – Detail of the bottom of the ADC layout: bottom of the resistive ladder, descodification of comparators 28 to 31 and output buffers (to pads).

Figure 8. – Detail of the top of the ADC layout: delay generator, enable, top of the resistive ladder, descodification of comparator 0.