An ISM 2.4 GHz Low-IF Receiver Frontend

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Abstract—This paper describes the implementation of an RF receiver frontend for the 2.4 GHz ISM band; it comprises an LNA, an IQ oscillator/mixer, and a low-pass filter. The proposed circuit is low cost and power efficient. To be low cost the circuit is inductorless and implemented in a standard nanoscale digital CMOS technology, with a state-of-the-art figure for area. To be power efficient all the circuits were chosen based on their power efficiency. A contribution in this paper is a new, more efficient, IQ oscillator/mixer block, where the current is reduced by 25% and reused for the two functions. A prototype of a low-IF receiver frontend is designed in UMC 130nm CMOS technology and simulated with a post-layout including pads netlist, and off-chip elements as bonding wires and load models. The frontend active area is 0.051 mm² (die area with pads is 0.395 mm²), and the power consumption is 16.3 mW from a 1.2 V supply for a frontend gain of 27 dB.

I. INTRODUCTION

Low cost (die area) and low power are key features in many simple applications, especially for disposable units, where a radio link comprising existing standards is not needed. The approach to realize low-cost RF circuits is to use a mainstream digital process (without expensive process options) and to design inductorless circuits, since they provide large savings in area (the complete circuit can be made smaller than a single integrated inductor) [1-2].

Inductorless circuits can exploit lumped circuit analog design procedures (avoiding microwave techniques). Circuits using these techniques can be tuned either digitally or by varying bias currents; they can also be more easily ported between applications and technologies. However, inductorless circuits usually have higher power consumption than tuned or resonant circuits with high quality factor passive components.

To mitigate this disadvantage the circuits here proposed use very efficient topologies taking advantage of structures with feedback. A new RC-oscillator circuit is here proposed which allowed a reduction in 25% on power consumption and a state-of-the-art figure-of-merit for this type of oscillators. This RC-oscillator is used in an IQ cross-coupled RC oscillator circuit where it is possible to implement the mixing directly, leading to further reduction in area and power consumption [3-4]. This circuit has very low phase mismatches because it employs feedback techniques, now possible to use in RF applications since mainstream CMOS technologies downscaling lead to transistor $f_T$ values in the order of tens of GHz.

In this work it is proposed a low-cost inductorless RF frontend for the non-proprietary Instrumental, Scientific and Medical (ISM) 2.4 GHz band, suitable for applications such as short distance medical monitoring and sensor networks.

This paper is organized in seven sections as follows. In section II the receiver frontend topologies are briefly described, emphasizing the restraints they impose on circuit specifications. In sections III to V the circuits are described, namely the LNA, the Oscillator/Mixer and the IQ Filter. In section VI it is presented a 2.4 GHz low-IF receiver frontend and its overall main specifications. Finally in section VII it is drawn the conclusions.

II. RECEIVER FRONTEND TOPOLOGY

A receiver (Rx) has a generic block diagram represented in Fig. 1. Its RF frontend main blocks are a low-noise amplifier (LNA), an oscillator (LO), a mixer and a filter (depending on the receiver topology a second oscillator and another filter can be used). Finally, the signal is converted to the digital domain by an analog-to-digital converter (ADC) for further processing.

There are two main topologies heterodyne (or IF) receivers where the signal is converted to an intermediate frequency (IF) or to more than one IF; and homodyne (or zero-IF) receivers where the signal is converted directly to the baseband frequency.

The heterodyne receiver main disadvantage is that, apart from the wanted signal, also an unwanted signal (image frequency signal) is converted to IF. This image signal has to be suppressed by an image reject filter before it is mixed down to the IF. Conventional heterodyne receivers require filter(s)

![Figure 1. Block diagram of a wireless receiver.](image-url)
with high quality factor difficult to comply for an integrated filter.

In the homodyne receiver the wanted signal is directly downconverted to baseband (the IF is zero) not requiring an image reject filter, a low-pass filter suffices. However it suffers from implementation problems as DC offsets, flicker noise and local oscillator leakage [5], which used to be severe restrictions for a practical implementation, but are now being overcome making this topology an interesting option.

The low-IF receiver – a special case of a heterodyne receiver- has recently been made possible with new circuit design techniques. In this type of receivers the RF signal is mixed down to a non-zero low or moderate intermediate frequency. It overcomes the disadvantages of the homodyne and of the conventional IF receivers. In low-IF receivers a local oscillator with high accurate quadrature outputs (Figure 1) is essential to remove the image frequency signal, [6].

In this work we have implemented a low-IF receiver in UMC 130nm CMOS technology and we have focused on the design of inductorless circuit blocks to achieve a very small area frontend.

III. LOW-NOISE AMPLIFIER (LNA)

A. LNA Topologies

The simplest way to match the LNA input impedance to the commonly used value of 50Ω is to put a resistance of the same value in parallel with the LNA input, but this incur in a 3 dB penalty in the noise figure (NF). Another most common topology is a common-gate stage where the input matching is obtained by the transistor transconductance reducing the penalty in the NF to approximately 2.2 dB. The most used topology is a common-source stage with inductive degeneration. Assuming that both, the transistor and the inductor, are ideally noiseless, it is possible to achieve real input impedance without any addition of noise. Moreover voltage gain and input matching are independent: transistor $g_m$ can be maximized to improve gain, while the values of $C_{gs}$ and $L_S$ are used to obtain the required input matching. These qualities make this topology very popular [5]. Its only drawback is the use of inductors, which have a large circuit area when compared to other components.

A common-source topology with resistive feedback in a shunt-shunt configuration as represented in Fig. 2 [7] is a compromise. For frequencies at which $sC_{gs}$ is negligible in comparison with $g_m$, the input impedance is almost real and equal to $1/g_m$ and if $g_m$ is high enough it is possible to have the voltage gain and the input impedance dimensioned almost independently.

![Figure 2. LNA with resistive feedback (biasing not represented).](Image)

Regarding the noise figure, the resistive feedback network generates thermal noise of its own. As a consequence, even ideally, the overall amplifier’s noise figure exceeds that of the common-source stage with inductive degeneration, while usually much better than the other mentioned topologies. Moreover, it is inductorless and it has all the advantages that come along from using a feedback loop: desensitization of the gain, lower nonlinear distortion and higher bandwidth.

B. Designed LNA

The LNA designed is the shunt-shunt topology represented in Fig. 3, it is a single-ended version of the LNA proposed in [8]. It can be divided in two main blocks: the amplifying block ($M_1, M_4$ and $R_D$) and the feedback block ($M_2$ and $R_{fb}$). $M_3$ and $M_5$ are used for biasing and to give extra circuit design variables, respectively.

The amplifier block is a cascode stage with a resistance load, where both transistors $M_1$ and $M_4$ must operate in the saturation region. The gain of this stage depends mainly on $g_{m1}$ and $R_D$. A cascode stage is used, to allow an extra degree of freedom in the design, together with $M_4$ (the current in $M_4$ can be increased without having a higher voltage drop in $R_D$, which could put $M_4$ out of the saturation region. The cascode also has other advantages such as higher gain, higher input-output isolation and larger bandwidth.

The feedback block is used to achieve the 50 Ω input matching. $M_5$ is used to permit adequate biasing of $M_2$.

![Figure 3. LNA Schematic.](Image)

The obtained simulation results are presented in Table I with and without buffer. It can be shown that the mixer capacitive load deteriorates the LNA performance, specially the $S_{11}$ parameter, therefore a common-drain stage is used as buffer. The buffer increases the power consumption but it ensures the wanted characteristics for the LNA.

<table>
<thead>
<tr>
<th>TABLE I. LNA RESULTS</th>
</tr>
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<tbody>
<tr>
<td></td>
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<tr>
<td>Current</td>
</tr>
<tr>
<td>$A_{vE} @ 2.4GHz$</td>
</tr>
<tr>
<td>$S_{11} @ 2.4GHz$</td>
</tr>
<tr>
<td>NF @ 2.4GHz</td>
</tr>
<tr>
<td>Bandwidth</td>
</tr>
</tbody>
</table>

IV. IQ OSCILLATOR/MIXER

For very demanding applications with high data rate and narrow channel spacing, LC oscillators are usually the first
choice for lower phase noise and lower power consumption. However, they use inductors with very large area (expensive) and usually require a frequency divider or an RC-CR network to obtain quadrature signals, which are open-loop topologies, where mismatches and other disturbances lead to quadrature error and reduce image rejection.

Cross-coupled RC oscillators are inductorless and can be implemented in the intended frequency range with wide tuning range. Coupling two cross-coupled RC oscillators generates accurate quadrature outputs and improves phase noise. It also makes the circuit robust to mismatches and other deviations while being capable of performing the mixer function in itself [3,4]. Some of these advantages are unique to this type of oscillators while reducing the gap in phase noise performance when compared with LC oscillators. In this paper a new RC oscillator circuit with reduced power consumption, that keeps the capability of performing the mixer function at no cost, is used.

![Figure 4. Low voltage and low power quadrature oscillator.](image)

The quadrature cross-coupled RC oscillator circuit proposed here, represented in Fig. 4, has two main differences when compared with the circuit in [3]: it has only one current source per single RC oscillator, current that is commuted ($M_{5/7}$-$M_{6/8}$) through the integrating capacitor at each half period (this would ideally reduce the power consumption by a factor of two); it has active coupling ($M_{9/10}$-$M_{11/12}$) circuits with a low voltage supply of 1.2 V, while most solutions to overcome such problem have used capacitive coupling. For a fair comparison the proposed circuit and a classic design were simulated in the same conditions (same frequency, same output voltage). To keep the circuits at the same frequency, it is necessary to have a current higher than the ideal value of 50%, since the capacitance at the integrator nodes change due to the extra parasitic capacitance of the switching transistors. A compromise reduction of 25% in the current was used but it also registered a phase-noise improvement of 3 dB which represent a gain of 4 dBc/Hz in the figures-of-merit (1)-(2).

\[
\text{FOM} = L_{\text{measured}} + 10\log\left(\frac{(\Delta f/f)^2}{\frac{P_{DC}}{P_{\text{ref}}}}\right) \quad (1)
\]

\[
\text{FOMA} = L_{\text{measured}} + 10\log\left(\frac{(\Delta f/f)^2}{\frac{P_{DC}}{P_{\text{ref}}}} A_{\text{chip}} \frac{A_{\text{ref}}}{A_{\text{chip}}}\right) \quad (2)
\]

where $\Delta f$ is the frequency deviation from the oscillation frequency $f$ in which the phase-noise ($L$) is measured, $P_{DC}$ is the power dissipated by the oscillator and $P_{\text{ref}}$ is a reference power level, typically 1 mW, $A_{\text{chip}}$ is the circuit area in mm$^2$ and $A_{\text{ref}}$ is a reference area (1 mm$^2$).

Simulation results are presented in Table II. The FOM and FOMA show state-of-the-art results for inductorless oscillators.

**TABLE II. SIMULATION RESULTS FOR QUADRATURE OSCILLATOR WITH BUFFERS, PADS AND BONDING WIRES, AND ESD PROTECTIONS.**

<table>
<thead>
<tr>
<th>Current [mA]</th>
<th>Freq [GHz]</th>
<th>PN [dBc/Hz] @1 MHz</th>
<th>PN [dBc/Hz] @3 MHz</th>
<th>PN [dBc/Hz] @10 MHz</th>
<th>FOM [dBc/Hz]</th>
<th>FOMA [dBc/Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.98</td>
<td>2.63</td>
<td>-90.05</td>
<td>-102.20</td>
<td>-114.20</td>
<td>-156</td>
<td>-173</td>
</tr>
</tbody>
</table>

V. **3rd ORDER $g_m$-C FILTER**

A 3rd order $g_m$-C Butterworth filter with cutoff frequency of 24 MHz is used to select the low-IF components at the Oscillator/Mixer outputs. The filter has two paths, I and Q, and each path has three stages: the filter itself, represented in Fig. 5; a differential-to-single ended stage; and an output buffer.

![Figure 5. 3rd Order $g_m$-C Filter.](image)

![Figure 6. $g_m$ cell schematic.](image)
The $g_m$ cell implemented is represented in Fig. 6 and the overall simulation results are presented in Table III. A pseudo-differential structure was chosen because it avoids the voltage drop across the tail current source and it can have a large signal swing with a low voltage supply. This pseudo-differential structure can be seen as the combination of two parallel transconductors with single ended output and, the output current is perfectly linear with respect to the input voltage if the transistors are kept in the saturation region [9].

TABLE III. SIMULATION RESULTS FOR 3RD ORDER $g_m$-C FILTER WITH BUFFERS, PADS AND BONDING WIRES, AND ESD PROTECTIONS.

<table>
<thead>
<tr>
<th></th>
<th>3rd Order $g_m$-C Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current [mA]</td>
<td>3.95</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>13.97</td>
</tr>
</tbody>
</table>

VI. 2.4 GHZ LOW-IF RECEIVER FRONTEND

The final results with simulations (extracted netlist) for the radio receiver are presented in Table IV and an input/output plot of a discrete signal Fourier transformation is shown in Figure 7, from where the overall gain can be calculated (-11.52 - (-39.01) = 27.5 dB). The radio receiver operates at 2.41 GHz and down-converts the input signals to 10 MHz. The receiver frontend layout is presented in Figure 8.

TABLE IV. SIMULATION RESULTS FOR THE COMPLETE LOW-IF RX.

<table>
<thead>
<tr>
<th></th>
<th>LNA</th>
<th>Buffer</th>
<th>Os/Mix</th>
<th>IQ Filter</th>
<th>Rx</th>
</tr>
</thead>
<tbody>
<tr>
<td>I [mA]</td>
<td>2.68</td>
<td>1.44</td>
<td>1.98</td>
<td>3.95</td>
<td>13.55</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>15.9</td>
<td>-2.92</td>
<td>1.15$^2$</td>
<td>13.97</td>
<td>27.5</td>
</tr>
<tr>
<td>Area[mm$^2$]</td>
<td>0.012</td>
<td>0.013</td>
<td>0.026</td>
<td>0.39$^3$</td>
<td></td>
</tr>
</tbody>
</table>

1 including references for the current mirrors.
2 voltage conversion gain: $V_{IFrms}/V_{RFrms}$, (IF@10 MHz, RF@2.41 GHz).
3 including pads.

All the circuits present competitive specifications at their class, resulting in a very compact and low-power design.

VII. CONCLUSIONS

In this work we present an RF frontend for the ISM frequency of 2.4 GHz. This receiver is intended for disposable applications where the most important specifications are cost and power consumption. The RF frontend is inductorless and comprises power efficient and low area circuits: LNA, IQ oscillator/mixer and IQ low-pass filters. The IQ oscillator is based on a new RC oscillator circuit which uses only one current source, becoming more efficient. The complete circuit active die area is only 0.05 mm$^2$ and the power consumption about 16.3 mW for a gain of 27 dB.

References