TÉCNICO LISBOA

Universidade de Lisboa

Curriculum Vitae of Professor

(First two pages *resume*)

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November 2015

Resume

Education

2004 Habilitation (Agregação) in Electrical and Computer Engineering (ECE), Instituto Superior Técnico (IST), Technical University of Lisbon (TU Lisbon), Portugal.

1996 PhD in Electrical and Computer Engineering, IST, TU Lisbon, Portugal.

1989 MSc in Electrical and Computer Engineering, IST, TU Lisbon, Portugal.

1984 Licenciatura (5 years) in Electronics and Telecommunications, Universid. de Aveiro, Portugal.

Positions and Experience

2017–*present* Head of the ECE Department at IST, Universidade de Lisboa.

2010–*present* Full Professor (Professor Catedrático) with the ECE Department at IST, Universidade de Lisboa.

2013–2016 Vice-President of the Scientific Council of IST, responsible for the PhD programs and research.

2009-2013 Chair of the Board of Directors of INESC-ID.

2008-2013 Director of the ECE BSc and MSc programs (2008-2013) and

1998–*present* Senior Researcher at INESC-ID.

Work Experience, Research Interests and Achievements

Supervised or co-supervised 15 PhD theses and more than 40 MSc theses, already finished.

Responsible for and taught at IST the courses "Advanced Computer Architecture", "Multimedia Architectures and Specialized Processors", "High Performance Computing Architectures" at the graduate level, and "Computer Electronics", "Electronics Systems for Signal Processing" at the undergraduate level.

Research interests include digital systems design and signal processing, architectures and circuits for general purpose and specialized processing, and high performance and parallel computing.

Principal investigator (PI) in 4 multiannual research projects funded by the Portuguese Foundation for Science and Technology and participated in more than 20 other funded research projects.

Participated in the evaluation committee and acted as an external reviewer of more than 50 PhD theses, in Portugal and in five other countries.

Contributed to more than 80 papers in scientific journals and 150 in international conferences, which receive a significant number of citations.

More than 30 invited invited talks given in universities, industries and conferences.

Professional Services

Associated Editor of the IEEE Transactions on Multimedia, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Access, Springer J. of Real-Time Image Processing and IET Electronics Letters

Editor in Chief of the EURASIP Journal on Embedded Systems, a SpringerOpen journal.

General-Chair of several Conferences, such as EUSIPCO 2014, HiPEAC WRC 2010, ISPDC 2009,

Program (Co-)Chair of IEEE BigMM 2017, IEEE ISM 2015, HeteroPar 2009, HiPEAC WRC 2009, SBAC-PAD 2014 ("Software"track), Euro-Par 2012 ("Scheduling and Load Balancing"topic), and SAMOS 2010 ("Applications, Systems, Architectures, and Processors"track).

Awards and Distinctions

2015 Selected ACM *Distinguished Scientist*.

2013 Elevated to Fellow of the IET.

2013, 2010 Best Paper and Poster Awards at the Conference on Design and Architectures for Signal and Image Processing (DASIP).

2011 "Stamatis Vassiliadis"Best Paper Award at the 11th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XI).

2010 Supervisor of the PhD thesis awarded with second placed in the **Fraunhofer Portugal Challenge**.

2009 Distinguished with an honorable mention for the impact of the publications in international scientific journals during the period 2004-2008 (award UTL/Santander Totta).

2008, 2004 Supervisor of the best MSc (2007/08) and Licenciatura (2003/04) theses at IST in the areas of Electrical and Computer Engineering and Informatics (award *Prof. Luís Vidigal*).

10 of the most important recent publications

2017 A. Ilic, F. Pratas and L. Sousa, "Beyond the Roofline: Cache-aware Power and Energy-Efficiency Modeling for Multi-cores", IEEE Transactions on Computers, vol. 66, n. 1, pp. 52-58.

2016 L. Sousa, S. Antão and P. Martins, "Combining Residue Arithmetic to Design Efficient Cryptographic Circuits and Systems", IEEE Circuits and Systems Magazine, vol. 16, n. 4, pp. 6-32.

2016 J. Andrade, G. Falcão, V. Silva and L. Sousa, "A Survey on Programmable LDPC Decoders,"IEEE Access, vol. 4, pp. 6704-6718.

2014 S. Momcilovic, A. Ilic, N. Roma and L. Sousa, "Dynamic load balancing for real-time video encoding on heterogeneous CPU+GPU systems," IEEE Transactions on Multimedia, vol. 16, no. 1, pp. 108– 121.

2014 A. Ilic, F. Pratas and L. Sousa, "Cache-aware roofline model: Upgrading the loft," IEEE Computer Architecture Letters, vol. 13, no. 1, pp. 21–24.

2011 G. Falcão, L. Sousa and V. Silva, "Massively LDPC decoding on multicore architectures," IEEE Transactions on Parallel and Distributed Systems (TPDS), vol. 22, no. 2, pp. 309—322.

2006 R. Chaves, G. Kuzmanov, L. Sousa and S. Vassiliadis, "Improving SHA-2 hardware implementations," in Proceedings of the Workshop on Cryptographic Hardware and Embedded Systems (CHES), Springer, LNCS, pp. 298–310.

2006 O. Sinnen, L. Sousa and F. Sandnes, "Towards a realistic task scheduling model," IEEE Transactions on Parallel and Distributed Systems, vol. 17, no. 3, pp. 263–275.

2005 O. Sinnen and L. Sousa, "Communication contention in task scheduling," IEEE Transactions on Parallel and Distributed Systems, vol. 16, no. 6, pp. 503–515.

2000 L. Sousa, "A general method for eliminating redundant computations in video coding," IEE Electronics Letters, vol. 36, no. 4, pp. 306–307.

1 Experience

Current Activities

Current position	Full Professor in the Electrical and Computer Engineering (ECE) Department at Instituto Superior Técnico(IST), Universidade de Lisboa (UL), in Portugal, since December 2010.
Teaching	Lecturer of basic and advanced courses on embedded systems, computer architectures, and parallel systems, included in the ECE M.Sc., and ECE and Computer Science Ph.D. programs at IST.
Research	Head a of a research group at *Instituto de Engenharia de Sistemas e Computadores, Investigação e Desenvolvimento* (INESC-ID), currently supervising 4 PhD students (supervised 14 PhD students that already finished), member of the EU FP7 Network of Excellence HiPEAC3, member of the management committee and Working Group Leader of the EU COST action Network for Sustainable Ultrascale Computing (NESUS), and Principal Investigator of the project *Stretching the Limits of Parallel Processing on Heterogenous Computing Systems* funded by the Portuguese Foundation for Science and Technology.
Conselor	One of the 14 members of the Scientific Council for Exact Sciences and Engineering of the Portuguese Foundation for Science and Technology (FCT), with the mission of providing the FCT Board with strategic advice and recommendations on developing, implementing and modifying science and technology in Portugal; Vice-Head of the Scientific Board of IST, a board composed by 20 elected members that plays a major role in the governance of IST.
Evaluator	Head of the National Panel for the final scientific evaluation of all projects in the area of Electrical Engineering funded by the FCT (2014-2016); evaluator of research project proposals of the H2020 program sponsored by the European Commission; reviewer and opponent on several these PhD defenses on international universities.
Speaker	Invited or keynote speaker on more than thirty conferences, universities and companies.
Professional service	Editor-in-Chief of the Springer EURASIP *Journal of Embedded Systems*, and Associate Editor of the IEEE *Transactions on Multimedia*, IEEE *Transactions on Circuits and Systems for Video Technology*, IEEE *Access*, and Springer *Journal of Real Time Image Processing*; involved in the organization of several international conferences (e.g. in 2014 in ICCD, SAMOS, Computing Frontiers, IPDPS, ICPP, Europar, EUSIPCO, SBAC-PAD); member of several international technical committees.

Previous Positions and Visiting Positions

Visit	Visiting Professor of the Electrical and Computer Engineering Department at Carnegie Mellon University, Pittsburgh, USA, Fall Semester 2016/2017. Faculty of Electrical Engineering, Mathematics and Computer Science of TU Delft (2002/03 spring semester).
Visit	JSPS Invitation Fellowship for Research in Japan (Short-term) and Visiting Professor of the Computer Science Departmente at the University of Tsukuba, Japan. "This fellowship program is to invite overseas researchers with excellent records of research achievements

for short-term visits to Japan and provide them opportunities for discussions, opinion exchanges, lectures and other activities". June-August 2016.

Positions — Chair of INESC-ID, a not for profit, privately owned institution of public interest, dedicated to advanced research and development in the domains of electronics, telecommunications and information technologies, with more than 100 PhD researchers and owned by IST (2009-2013); Coordinator of the M.Sc. and B.Sc. programs in ECE at IST, which totalize more than 1500 students (2008-2012).

Visit — Visiting Professor in the Computer Engineering Lab at the Faculty of Electrical Engineering, Mathematics and Computer Science of TU Delft (2002/03 spring semester).

2 Academic Degrees

- Habilitation (Agregação in Portugal) in Electrical and Computer Engineering, at IST, in 2004. *Thesis title*: Architectures and Algorithms for Signal Processing in Real Time.
- Ph.D. degree in Electrical and Computer Engineering, at IST, in 1996. *Thesis title*: Parallel Image Processors with Orthogonal Access to Shared Memory.
- M.Sc. in Electrical and Computer Engineering, at IST, in 1989. *Thesis title*: Algorithms and Architecture for the Digital Signal Processing System APICE.
- Licenciatura in Electronics and Telecommunications at University of Aveiro, in 1984.

3 Teaching

My teaching experience comprises: the development of new advanced postgraduate courses in the area of Computer Engineering; the coordination, for five years, of the MSc and BSc programs in Electrical and Computer Engineering (ECE) at IST, with a total of more than 1500 students; and the teaching of courses in this area. I have developed pedagogical material to the courses that I taught, which has been used through the years.

Teaching — I have taught courses on Computer Organization, Computer Architecture, Embedded Systems, and Parallel Computing Architectures over the past 15 years. Notwithstanding I have introduced several courses in the M.Sc. and Ph.D. ECE programs, I have also taught courses on Embedded Systems, namely the *Computer Electronics* course and the *Basic Electronics* courses.

New courses — I have designed and introduced the following new courses in the IST MS.C and Ph.D. Programs in ECE: *Advanced Computer Architectures*, started in 2003/2004 and has been running in the M.Sc. program all spring semesters; *Specialized Digital Processors*, launched as an elective course in 1997/98 and offered in the program till 2002/2003; and *High Performance Computing Architectures*, a course that is running in the PhD program since 2006/2007. I have developed advanced lab tutorials for courses in computer architecture and embedded systems, an example can be found in *A Lab Project on the Design and Implementation of Programmable and Configurable Embedded Systems*, one of the most popular articles of the *IEEE Transactions on Education*.

Curriculum Design — I was also involved in curriculum design, 2006/2007, on adapting the ECE integrated M.Sc. Program according to the Bologna declaration. Being in charge of coordinating the M.Sc. and

the B.Sc. ECE programs in IST since 2009, in 2011/2012 I redesigned the ECE M.Sc. Program, namely the organization of the specialization areas and the courses offered in each one of those areas.

Textbooks — I am co-author of the textbook *Bioelectronic Vision Retina Models, Evaluation Metrics, and System Design*, series on Bioengineering and Biomedical Engineering, vol. 3, World Scientific, a textbook for advanced undergraduate and graduate students in biomedical engineering, and electrical and computer engineering. This book provides a technical perspective of the functional and structural retina models, and provides insight about the models used on hardware implementations.

4 Research Focus and Achievements

The focus of my research has been on computer architecture and high performance computing, namely the design of highly efficient architectures, algorithms and circuits for current and emergent applications. My research work has evolved by taking a holistic system perspective that addresses the interaction between applications, algorithms, software and hardware platforms, and how it impacts the performance and tradeoffs across different hardware and software solutions. Among others, there are two key topics in which I have made cutting-edge research contributions: Hardware Accelerators, and Parallel Heterogeneous Systems.

- *Parallel Heterogeneous Systems*
  - Communication-aware static task scheduling algorithms for multicore and distributed systems: in a ground work, it was shown the impact of communication for task scheduling in cluster systems [**?**], and new system model and scheduling algorithms were proposed [**?**]. These contributions have a significant impact in static task scheduling and they represent an unavoidable research basis for current scientific studies in parallel and distributed systems (more than 250 citations in the Scholar).
  - Insightful performance modeling of multi-core architectures: this recent contribution tackles the important topic of roofline modeling for multi-cores (very much used, more than 100 citations just in 2014). To overcome serious limitations of the original model, the Cache-Aware Roofline Model (CARM) [**?**] explicitly considers a complete memory hierarchy when describing the performance of multi-core architectures.
  - On-the-fly performance modeling and dynamic load balancing for heterogeneous systems: these contributions also led to development of several on-the-fly performance modeling and scheduling algorithms for heterogeneous multi-core systems, namely for parallel CPU+GPU systems and highly heterogeneous multi-cluster environments; these algorithms have been applied for a plethora of different applications, such as video encoding, data-base applications, linear algebra and digital signal processing [**?**, **?**], [**?**].
- *Hardware Accelerators*
  - Pioneer work on programming models and tools for stream-based computing, when in early 2000's, GPU programming and execution models were proposed for the first time (as the forerunners to nowadays common concepts), e.g. *flow-model* for stream computing and the programming tool and run-time system Caravela [**?**], with its extension to GPU-based distributed computing [**?**]. This work opened gates to the use of GPUs beyond their graphics purposes, e.g., for solving regular and irregular Low-Density Parity-Check (LDPC) [**?**, **?**], [**?**, **?**].

– Theoretical formulation of computational redundancy in predictive video coding approaches [**?**]: served as the basis for further investigation and practical application to exploit redundancy in all current video encoding standards Discrete Cosine Transform (DCT) based or integer DCT-based transforms [**?**].

– Design of specific programmable and dedicated accelerators, mostly for signal processing and cryptography: fully exploiting data and spatial parallelism [**?**] [W.16] [**?**] and also parallelism at arithmetic level, for example by investigating Residue Number Systems (RNS) based parallel cryptographic systems [**?**, **?**], and energy-efficiency in embedded systems [**?**] [**?**].

5 Publications

190 publications in DBLP, more than 1400 citations registered in Scopus (h-index 19), and more than 3000 in the Google Scholar (h-index 27), the most relevant are listed below.

5.1 Textbook

[B.1] J. Martins and L. Sousa, *Bioelectronic Vision: Retina Models, Evaluation Metrics, and System Design*, volume 3 of *Series on Bioengineering & Biomedical Engineering*, World Scientific, London, March 2009.

5.2 Journal papers

5.3 Conference papers (refereed)

5.4 Workshop papers (refereed)

[W.1] S. Momcilovic, N. Roma and L. Sousa, "Multi-level parallelization of advanced video coding on hybrid CPU+GPU platforms," in *International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar)*, August 2012.

[W.2] A. Ilic and L. Sousa, "Simultaneous multi-level divisible load balancing for heterogeneous desktop systems," in *ISPA 2012, International Workshop on Heterogeneus Architectures and Computing*, March 2012, pp. 683–690.

[W.3] A. Ilic and L. Sousa, "Scheduling divisible loads on heterogeneous desktop systems with limited memory," in *Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar)*, July 2011.

[W.4] P. Petrides, F. Pratas, L. Sousa and P. Trancoso, "Virtualization for morphable multi-cores," in *Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures*, January 2011.

[W.5] R. Ramalho, P. Tomás and L. Sousa, "Efficient independent component analysis on a GPU," in *Proceedings of the International Workshop on Frontier of GPU Computing (FGC)*, IEEE Computer Society Press, July 2010.

[W.6] A. Rodrigues, N. Roma and L. Sousa, "p264: Open platform for designing parallel H.264/AVC video encoders on multi-core systems," in *Proceedings of the International Workshop on Network and Operating Systems Support for Digital Audio and Video (NOSSDAV)*, ACM, June 2010, pp. 81–86.

[W.7] A. Ilic and L. Sousa, "Collaborative execution environment for heterogeneous parallel systems," in *Proceedings of the 12th Workshop on Advances in Parallel and Distributed Computational Models (APDCM/IPDPS 2010)*, May 2010.

[W.8] F. Pratas, R. Mata and L. Sousa, "Iterative induced dipoles computation for molecular mechanics on GPUs," in *Proceedings of the 3rd Workshop on General Purpose Processing on Graphics Processing Units (co-located with ASPLOS)*, ACM, February 2010, pp. 111–120.

[W.9] S. Momcilovic and L. Sousa, "Development and evaluation of scalable video motion estimators on GPU," in *Proceedings of the Workshop on Signal Processing Systems (SiPS)*, IEEE, October 2009, pp. 291–296.

[W.10] F. Pratas and L. Sousa, "Applying the stream-based computing model to design hardware accelerators: A case study," in *Proceedings of the International Workshop on Systems, Architectures, Modeling, and Simulation*, Springer, July 2009, LNCS, pp. 237–246.

[W.11] T. Tulabandhula, S. Antão and L. Sousa, "A class of software-hardware processors for fingerprint matching on the fourier domain," in *Proceedings of the 3rd HiPEAC Workshop on Reconfigurable Computing*, January 2009.

[W.12] S. Yamagiwa and L. Sousa, "Design and implementation of a tool for modeling and programming deadlock free meta-pipeline applications," in *Proceedings of the 10th Workshop on Advances on Parallel and Distributed Processing Symposium (APDCM/IPDPS)*, IEEE, April 2008.

[W.13] S. Momcilovic and L. Sousa, "A parallel algorithm for advanced video motion estimation on multi-core architectures," in *Proceedings of the International Workshop on Multi-Core Computing Systems (MuCoCoS)*, IEEE, March 2008, pp. 831–836.

[W.14] G. Fernandes, S. Yamagiwa, V. Silva and L. Sousa, "Stream-based LDPC decoding on GPUs," in *Proceedings of the First Workshop on General Purpose Processing on Graphics Processing Units*, September 2007.

[W.15] S. Momcilovic, N. Roma and L. Sousa, "An ASIP approach for adaptive motion estimation on AVC," in *Proceedings of the IEEE 3rd Conference on PhD Research in Microelectronics and Electronics (PRIME)*, July 2007, pp. 165–168.

[W.16] R. Chaves, G. Kuzmanov, L. Sousa and S. Vassiliadis, "Improving SHA-2 hardware implementations," in *Proceedings of the Workshop on Cryptographic Hardware and Embedded Systems (CHES)*, Springer, October 2006, LNCS, pp. 298–310.

[W.17] T. Dias, N. Roma and L. Sousa, "Low power distance measurement unit for real-time hardware motion estimators," in *Proceedings of the International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, Springer, September 2006, volume 4148 of *Lecture notes in Computer Science*, pp. 247–255.

[W.18] R. Chaves, G. Kuzmanov, L. Sousa and S. Vassiliadis, "Rescheduling for optimized SHA-1 calculation," in *Proceedings of the SAMOS Workshop on Computer Systems Architectures Modelling and Simulation*, Springer, July 2006, volume 4017 of *LNCS*, pp. 425–434.

[W.19] R. Chaves, G. Kuzmanov, S. Vassiliadis and L. Sousa, "Reconfigurable memory based AES co-processor," in *Proceedings of IEEE 20th International Parallel & Distributed Processing Symposium, 13th Reconfigurable Architectures Workshop*, IEEE Computer, April 2006.

[W.20] R. Piedade and L. Sousa, "Configurable embedded core for controlling electro-mechanical systems," in *Proceedings of the Applied Reconfigurable Computing Workshop (ARC)*, Springer Verlag, February 2006, volume 3985 of *Lecture notes on Computer Science*, pp. 18–23.

[W.21] T. Dias, N. Roma and L. Sousa, "Efficient motion vector refinement architecture for sub-pixel motion estimation systems," in *Proceedings of IEEE Workshop on Signal Processing Systems (SiPS)*, Atenas, Grécia, November 2005, pp. 313–318.

[W.22] O. Sinnen and L. Sousa, "Task scheduling: Considering the processor involvement in communication," in *Proceedings of the IEEE International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Networks (HeteroPar)*, Cork, Irlanda, July 2004, pp. 328–335.

[W.23] O. Sinnen and L. Sousa, "Comparison of contention aware list scheduling heuristics for cluster computing," in *Proceedings of the Workshop on Scheduling and Resource Management for Cluster Computing (ICPP)*, IEEE Computer Society Press, Valência, Espanha, September 2001, pp. 382–387.

[W.24] N. Roma and L. Sousa, "Parameterizable hardware architectures for automatic synthesis of motion estimation processors," in *Proceedings of IEEE Workshop on Signal Processing Systems (SiPS)*, Antuérpia, Bélgica, September 2001, pp. 428–439.

[W.25] N. Roma and L. Sousa, "On the development and evaluation of specialized processors for computing high-order 2-D image moments in real-time," in *Proceedings of the International Workshop on Computer Architectures for Machine Perception*, IEEE, Padova, Itália, September 2000, pp. 170–179.

[W.26] J. Brito and L. Sousa, "A video codec based on the TMS320C6X DSP," in *Proceedings of the European DSP Education and Research Conference*, Texas Instruments, Paris, França, September 2000.

[W.27] L. Sousa and N. Roma, "On the design of low-power array architectures for motion estimation," in *Proceedings of the IEEE 3rd Workshop on Multimedia Signal Processing*, Copenhaga, Dinamarca, September 1999, pp. 679–684.

[W.28] A. Abreu, N. Roma, J. Gerald and L. Sousa, "Digital video transmission through the electrical power lines," in *Proceedings of the European DSP Education and Research Conference*, Texas Instruments, Paris, França, September 1998, pp. 16–21.

[W.29] A. Costa, J. Bárrios, L. Sousa and M. Piedade, "Low and intermediate parallel image processing for transputer base systems," in *Proceedings of the European Workshops on Parallel Computing*, Barcelona, Espanha, March 1992, pp. 393–396.

[W.30] O. Mealha, J. Delgado and L. Sousa *et al*, "PARSEC-parallel computing in signal processing and environments for concurrent systems," in *Proceedings of the Second Workshop of the Parallel Computing Action*, Directorate General XXIII, Commission of the European Communities, December 1990, pp. 378–395.

5.5 Book Chapters

[BC.1] N. Pinckney, D. Harris, N. Jiang, K. Kelley, S. Antao and L. Sousa, *Circuits and Systems for Security and Privacy*, CRC Press, chapter Public Key Cryptography, pp. 109–182, May 2016.

[BC.2] R. Chaves, L. Sousa, N. Sklavos, A. Fournaris, G. Kalogeridou, P. Kitsos and F. Sheikh, *Circuits and Systems for Security and Privacy*, CRC Press, chapter Secure Hashing: SHA-1, SHA-2, and SHA-3, pp. 81–107, May 2016.

[BC.3] J. Andrade, G. Falc ao, V. Silva, S. Yamagiwa and L. Sousa, *Encyclopedia of Computer Science and Technology*, Taylor and Francis Group, chapter Accelerating Conventional Processing Using GPU Clusters: LDPC Decoders, 2015.

[BC.4] L. Kuan, P. Tomás and L. Sousa, *Numerical Computations with GPUs*, Springer, chapter Finite-Difference in Time-Domain scalable implementations on CUDA and OpenCL, July 2014.

[BC.5] A. Ilic and L. Sousa, *High-Performance Computing on Complex Environments*, Wiley, chapter 14: Efficient Multilevel Load Balancing on Heterogeneous CPU + GPU Systems, pp. 261–279, June 2014.

[BC.6] D. Clarke, A. Ilic, A. Lastovetsky, V. Rychkov, L. Sousa and Z. Zhong, *High-Performance Computing on Complex Environments*, Wiley, chapter 13: Design and Optimization of Scientific Applications for Highly Heterogeneous and Hierarchical HPC Platforms Using Functional Computation Performance Models, pp. 237–257, June 2014.

[BC.7] S. Ant ao, R. Chaves and L. Sousa, *Embedded Systems: Hardware, Design and Implementation*, John Wiley & Sons, chapter 14: Reconfigurable Architecture for Cryptography over Binary Finite Fields, pp. 319–362, January 2013.

[BC.8] A. Ilic, F. Pratas, P. Trancoso and L. Sousa, *High Performance Computing: From Grids and Clouds to Exascale*, IOS Press, chapter High-Performance Computing on Heterogeneous Systems: Database Queries on CPU and GPU, pp. 202–222, September 2011.

[BC.9] P. Tomás, A. Ilic and L. Sousa, *Biomedical Diagnostics and Clinical Technologies: Applying High-Performance Cluster and Grid Computing*, IGI Global, chapter 9: Massive Data Classification of Neural Responses, February 2010.

[BC.10] G. Falc ao, V. Silva and L. Sousa, *GPU Computing Gems*, Morgan Kaufmann, chapter 39: Parallel LDPC Decoding, December 2010.

[BC.11] Gabriel Falc ao, Vitor Silva, José Marinho and Leonel Sousa, *WIMAX New Developments*, IN-TECH, chapter 6: LDPC Decoders for the WiMAX (IEEE 802.16e) based on Multicore Architectures, pp. 133–150, December 2009.

[BC.12] M. Piedade, J. Gerald, L. Sousa and G. Tavares, *VLSI Circuits for Biomedical Applications*, Artech House, chapter 2: Visual Cortical Neuroprosthesis: A System Approach, pp. 25–43, April 2008.

[BC.13] S. Yamagiwa and L. Sousa, *Concurrent & Parallel Computing: Theory, Implementation and Applications*, Nova Science Publishers, chapter 1. Caravela: A High Performance Stream-based Concurrent Computing Platform, pp. 1–37, 2008.

[BC.14] N. Roma, T. Dias and L. Sousa, *New Algorithms, Architectures and Applications for Reconfigurable Computing*, Lysaght P. e Rosenstiel W. (Eds.), Springer-Verlag, chapter 5. Customisable and Reduced Hardware Motion Estimation Processors, pp. 55–66, 2005.

[BC.15] L. Sousa, P. Tomás, F. Pelayo, A. Martinez, C. Morillas and S. Romero, *New Algorithms, Architectures and Applications for Reconfigurable Computing*, Lysaght P. e Rosenstiel W. (Eds.), Springer-Verlag, chapter 22. Bioinspired Stimulus Encoder for Cortical Visual Neuroprostheses, pp. 279–290, 2005.

[BC.16] L. Sousa and N. Roma, *SOC Design Methodologies*, Kluwer Academic Publishers, volume 218 of *IFIP International Federation for Information Processing*, chapter A New VLSI Architecture for Full Search Block Matching Motion Estimation, pp. 253–264, 2002.

[BC.17] L. Sousa and M. Piedade, *Parallel Algorithms for Digital Image Processing, Computer Vision and Neural Networks*, Ioannis Pitas (Ed.), John Wiley & Sons, Nova Iorque, chapter Low Level Parallel Image Processing, pp. 25–52, 1993.

5.6 Edited Books, Proceedings, and Special Issues

[E.1] Amir Molahosseini, Leonel Sousa and Chip Hong Chang (eds.), *Embedded Systems Design with Special Arithmetic and Number Systems*, Springer, 2016, in Press.

[E.2] Farhana Sheikh and Leonel Sousa (eds.), *Circuits and Systems for Security and Privacy*, CRC Press, May 2016, ISBN 9781482236880.

[E.3] YongHong Tian, Min Chen and Leonel Sousa (eds.), *Ubiquitous Multimedia: Emerging Research on Multimedia Computing*, volume 23, IEEE MultiMedia, February 2016.

[E.4] Min Chen, Leonel Sousa and YongHong Tian (eds.), *Special Issue of ISM'16*, volume 10, Int. J. Semantic Computing, August 2016.

[E.5] Leonel Sousa and Nuno Roma (eds.), *Special Issue The Circuits and Systems for HEVC and 3D/SVC*, Journal of Real Time Image Processing, Springer, 2016.

[E.6] Y. Robert, Leonel Sousa and Denis Trystram (eds.), *Special Issue Follow-on of ISPDC'2009 and HeteroPar'2009*, volume 37, Parallel Computing, Elsevier, August 2011.

[E.7] H. Lin, M. Alexander, M. Forsell, A. Knüpfer, R. Prodan, L. Sousa and A. Streit (eds.), *Euro-Par 2009 - Parallel Processing Workshops*, volume 6043 of *Lecture Notes in Computer Science*, Springer, June 2010.

[E.8] L. Sousa and Yves Robert (eds.), *Proceedings of the Eighth International Symposium on Parallel and Distributed Computing*, IEEE Computer Society, July 2009, ISBN 978-0-7695-3680-4.

[E.9] L. Sousa, N. O'Connor, M. Mattavelli and A. Nunez (eds.), *EURASIP Journal of Embedded Systems*, Editor responsável pelo número especial em *Embedded Systems for Portable and Mobile Video Platforms*, February 2007.

6 Supervision Ph. D. and (before Bologna) Master Theses

6.1 PhD Theses

2016 Lídia Kuan, "Exploiting Parallel Heterogeneous Systems for Scientific Computations", Electrical and Computer Engineering Department (DEEC), IST (co-supervisor). First Employment: RiskCo, Portugal.

2015 Tiago Dias, "High Performance and Scalable Unified Architectures for Transform and Quantization in H.264/AVC Codecs", Electrical and Computer Engineering Department (DEEC), IST (co-supervisor). First Employment: Instituto Politécnico de Lisboa, Portugal.

2015 Pedro Matutino, "Residue Number Systems: Efficient Architectures and Circuits", Electrical and Computer Engineering Department (DEEC), IST. First Employment: Instituto Politécnico de Lisboa, Portugal.

2014 Aleksandar Ilic, "Heterogeneous Systems: Load Balancing and Performance Modeling", Electrical and Computer Engineering Department (DEEC), IST. First Employment: Pos-Doc at INESC-ID, Portugal.

2013 Samuel Antão, "High-performance and Embedded Systems for Cryptography", Electrical and Computer Engineering Department (DEEC), IST. First Employment: IBM Thomas J. Watson Research Center, NY, USA.

2013 João Martins, "Computational Models, Neuronal Metrics and System Identification in Bioelectronic Vision", (main advisor, co-advisor Prof. José Caeiro) Electrical and Computer Engineering Department (DEEC), IST. First Employment: Instituto Politécnico de Beja, Portugal.

2012 Frederico Pratas, "Stream-based Computing and Fine-grained Parallelism: from Algorithms to Reconfigurable Hardware", (main advisor, co-advisor Prof. Pedro Trancoso) Electrical and Computer Engineering Department (DEEC), IST. First Employment: Intel Labs Barcelona (ILBA), Spain.

2011 José Germano, "A Hand-held Microsystem for Biological Analysis: Electronics, Signal Acquisition and Processing for Information Extraction", Electrical and Computer Engineering Department (DEEC), IST. First Employment: Post-Doc at INESC-ID, Portugal.

2011 José Sarmento, "Optimized Digital Clock and Data Recovery Architectures", DEEC, IST. First Employment: Synopsis Portugal.

2011 Svetislav Momcilovic, "Parallel Video Coding on Multicore Platforms", DEEC, IST. First Employment: Post-Doc at INESC-ID, Portugal.

2010 Gabriel Fernandes, "Parallel Algorithms and Architectures for LDPC Decoding"(main advisor, co-advisor Prof. Vitor Silva), Electrical and Computer Engineering Department, Universidade de Coimbra. First Employment: Assistant Professor at Universidade de Coimbra.

2009 Pedro Tomás, "Neural Code: Tunning and Assessment of Retina Models", DEEC, IST. First Employment: Assistant Professor at DEEC, IST.

2008 Nuno Roma, "Transform domain video transcoding systems for static and dynamic video composition", DEEC, IST. First Employment: Assistant Professor at the Informatics and Computer Engineering Department (DEIC), IST.

2007 Ricardo Chaves, "Secure Computing on Reconfigurable Systems"(co-advisor), Faculty Electrical Engineering, Mathematics and Computer Science, Technical University of Delft. First Employment: Assistant Professor at the Informatics and Computer Engineering Department (DEIC), IST.

2003 Oliver Sinnen, "Accurate Task Scheduling for Parallel Systems", DEEC, IST. First Employment: Lecturer at the Department of Electrical and Computer Engineering (ECE), University of Auckland, New Zealand.

6.2 Master Theses (before-Bologna, half-way between MSc. and Ph. D.)

2007 Sérgio Martins, "Non-Linear Functionals for Retina Models", Master in Electrical and Computer Engineering, IST.

2007 Sérgio Capela, "Stochastic Integrate-and-Fire Retina Model", Master in Electrical and Computer Engineering, IST.

2007 Miguel Nuno Ribeiro, "A Configurable Processing Platform and its Application to Video Coding", Master in Electrical and Computer Engineering, IST.

2006 João Martins, "Computational Retina Models for Bioelectronic Vision", Master in Electrical and Computer Engineering, IST.

2006 Gustavo Rocha, "Graph Generation from Software Descriptions", Master in Electrical and Computer Engineering, IST.

2005 José Germano , "Portable System for DNA Analysis based on a Biochip"(co-supervised with Prof. Moisś Piedade), Master in Electrical and Computer Engineering, IST.

2005 Pedro Tomás, "Algorithms and Tools for Automatic Generation of DSP Hardware Structures", Master in Electrical and Computer Engineering, IST.

2004 Ricardo Guapo, "Programming and Evaluation of the Berkeley Socket Interface on the Maestro2 Communication System", Master in Electrical and Computer Engineering, IST.

2003 Tiago Dias, "High Performance VLSI Motion Estimation Processors: Data Reuse and Sub-Pixel Accuracy", Master in Electrical and Computer Engineering, IST.

2002 Ricardo Chaves, "RDSP: Processador Digital de Sinal com Suporte para Aritmética por Resíduos"(thesis written in portuguese), Master in Electrical and Computer Engineering, IST.

2002 José Salvado, "Codificação de Vídeo por Decomposição 3D baseada na Transformada de Ôndulas"(thesis written in portuguese), Master in Electrical and Computer Engineering, IST.

2001 Oliver Sinnen, "Experimental Evaluation of Task Scheduling Accuracy", Master in Electrical and Computer Engineering, IST.

2000 Nuno Roma, "Processadores Dedicados para Estimação de Movimento em Sequências de Vídeo"(thesis written in portuguese), Master in Electrical and Computer Engineering, IST.

7 Professional Services

7.1 Involvement on scientific and technical strategic discussions

2016 State of the Art and Research Roadmap for NESUS-WG1

2016 Co-organizer of the Tematic Session "Industry Activities related to Computing Systems in Portugal"as part of the programme of the Computing System Week (CSW) of the HiPEAC European Network of Excellence, Porto.

2015 Panelist in the panel "(Micro)Electronics Industry and University - interfaces questioned"in the *XXX Conference on Design of Circuits and Integrated Systems*, November in Estoril, Portugal, together with Michel Renovell, Antonio Torralba, Teresa Riesgo and Nuno Paulino.

2008 Participation in the Round table discussion: "Parallel and Distributed Computing in the Chip Multi-Processor System Era", in the *7th International Symposium on Parallel and Distributed Computing*, July in Krakow, Poland, together with Michael J. Flynn, Dean Tullsen and John Morrison.

2006 Involvement in the preparation of the document of the Thematic Group 7 "Tera-Device Computing and Beyond", which provides the European Commission with the vision, and also the major challenges

of computer engineering in Europe.

7.2 Editorial Services

2016 IEEE Transactions on Multimedia (TMM) Best Paper Award Selection Committee.

2016 Guest Co-Editor for the Special Issue of the IEEE Multimedia on "Ubiquitous Multimedia: Emerging Research on Multimedia Computing", with Min Chen and Yonghong Tian.

2016 Guest Co-Editor for the Special Issue of the International Journal of Semantic Computing (IJCS), extended best papers from ISM'2015, with Min Chen and Yonghong Tian.

2016 Guest Editor for the Special Issue of the Springer Journal of Real-Time Image Processing on "Real-Time Energy-Aware Circuits and Systems for HEVC and for its 3D and SVC Extensions", with Nuno Roma.

2015- Editor-in-Chief of the EURASIP Journal on Embedded Systems (JES), SpringerOpen Journal.

2015- Associate Editor and Member of the Editorial Board of the IET Electronics Letters.

2015 Nominated by the IEEE Computer Society Technical Committee on Multimedia Computing (TCMC) for the committee to select Special Issues and Survey/overview proposals to the IEEE Transactions on Multimedia (TMM).

2015 IEEE Transactions on Multimedia (TMM) Best Paper Award Selection Committee.

2014- Associate Editor and Member of the Editorial Board of the IEEE Transactions on Multimedia (TMM).

2014- Associate Editor and Member of the Editorial Board of the IEEE Transactions on Circuits and Systems for Video Technology (TCSVT).

2014- Associate Editor of the IEEE *Access*.

2013- Associate Editor of the Journal of Real-Time Image Processing, Springer.

2005-2014 Associate Editor of the EURASIP Journal on Embedded Systems (JES), SpringerOpen Journal.

2011 Guest editor for "Follow-on of ISPDC'2009 and HeteroPar'2009", volume 37, number 8 of the *Parallel Computing* journal, Elsevier, together with Y. Robert and Denis Trystram.

2010 Editor for "Euro-Par 2009 - Parallel Processing Workshops", Lecture Notes in Computer Science, volume 6043, Springer, together with H. Lin, M. Alexander, M. Forsell, A. Knüpfer, R. Prodan and A. Streit.

2009 Editor of the "Proceedings of the Eighth International Symposium on Parallel and Distributed Computing", IEEE Computer Society, with Yves Robert.

2007 Guest editor for "Embedded Systems for Portable and Mobile Video Platforms", special issue of the EURASIP Journal on Embedded Systems, together with N. O'Connor, M. Mattavelli and A. Nunez.

7.3 Chairmanship, and Steering Committee Appointments

2017 Program Co-Chair of the IEEE 3rd International Conference on Multimedia Big Data (BigMM 2017), California, USA.

2016 Publicity Committee Co-Chair of the IEEE International Symposium on Multimedia, San Jose, California, USA.

2015 Program Co-Chair of the IEEE International Symposium on Multimedia, Miami, Florida, USA.

2015 Co-Chair of the Special Session of ISCAS'15 on "Special Session on "Efficient Circuits and Systems for HEVC and its 3D Encoding Extension", Lisboa, Portugal.

2014 General Chair of 22th European Signal Processing Conference (EUSIPCO), EURASIP, Lisboa, Portugal.

2014 Track Chair of the the 25th International Symposium on Computer Architecture and High Performance Computing, Paris, France.

2013 Program Co-Chair of The Workshop on Power and Energy Aspects of Computation, co-located with the 10th International Conference on Parallel Processing and Applied Mathematics (PPAM), Warsaw, Poland.

2011 General Chair of Topic 3, *Scheduling and Load Balancing*, Euro-Par, Bordeaux, France.

2010 Co-Chair of The Applications, Systems, Architectures, and Processors Track, of the International Symposium on Systems, Architectures, MOdeling and Simulation, (IC-SAMOS), IEEE, Samos, Greece.

2010 General Co-Chair of the 4th HiPEAC Workshop on Reconfigurable Computing (WRC), co-located with the International Conference on High Performance Embedded Architectures & Compilers, Pisa, Italy.

2009 General Chair of the 8th International Symposium on Parallel and Distributed Computing (ISPDC), Lisboa, Portugal.

2009 Program Chair of the International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Networks (HeteroPar), co-located with Euro-Par, Delft, Netherlands.

2009 Program Co-Chair of the 3rd HiPEAC Workshop on Reconfigurable Computing, co-located with the International Conference on High Performance Embedded Architectures & Compilers, Paphos, Cyprus.

2011- Member of the Advisory Board of the EuroPar.

2010- Member of Steering Committee of the International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar).

2008-2011 Member of Steering Committee of the International Symposium on Parallel and Distributed Computing (ISPDC).

2008 International Liaison Co-Chair of the 5th International Conference on Ubiquitous Intelligence and Computing, Oslo, Norway.

7.4 Program Committee Membership

I have served on more than 100 Program and Technical Committees of Conferences and Workshops, some of the most relevant are listed below.

- IEEE IPDPS (International Parallel and Distributed Processing Symposium): 2014, 2013, 2012, 2010, 2007, 2003.
- IEEE International Conference on Computer Design (ICCD): 2015, 2014, 2013, 2012, 2011, 2010.
- IEEE/ACM International Conference on High Performance Computing (HiPC): 2016, 2015, 2014, 2012, 2011, 2010.
- ACM International Conference on Computing Frontiers: 2017, 2016, 2015, 2014, 2011
- IEEE International Conference on Parallel and Distributed Systems (ICPADS): 2008, 2006.
- International Conference on Parallel Processing (ICPP): 2014-2011.
- ACM International Conference on Supercomputing (ICS): 2006.
- IEEE International Symposium on Systems, Architectures, MOdeling and Simulation Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS): 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009.
- Euro-Par: 2015, 2014, 2011.
- International Conference on Architecture of Computing Systems (ARCS): 2017, 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009.
- Euromicro Conference on Digital System Design: Architectures Methods and Tools (DSD): 2016-2010.
- International Symposium on Parallel and Distributed Computing (ISPDC): 2016-2009.
- International Conference on Parallel Processing and Applied Mathematics (PPAM): 2017, 2015, 2013, 2011, 2009.
- The First IEEE International Conference on Multimedia Big Data (BigMM): 2016, 2015
- IEEE International Symposium on Multimedia (ISM): 2015, 2014
- Wireless Innovation Forum Conference on Communications Technologies and Software Defined Radio (WinnComm): 2016, 2015, 2014, 2013
- 12th International Meeting on High Performance Computing for Computational Science (VECPAR): 2016
- IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), track "Design and Implementation of Signal Processing Systems (DISPS)": 2016
- IEEE International Workshop on Signal Processing Systems (SiPS): 2016.
- HiPEAC Workshops WRC, PARMA-DITAM, and CS2 co-located with the HiPEAC conference: 2016-2014.

7.5 Reviewing for Scientific Journals and Textbooks

- Referee for the IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Transactions on Circuits and Systems I: Regular Papers, IEEE Transactions on Circuits and Systems II: Express Briefs, IEEE Transactions on Signal Processing, IEEE Signal Processing Letters, IEEE Signal Communication Letters, ACM Journal of Experimental Algorithmics, IET Electronics Letters, IET Image Processing, IET Circuits, Devices & Systems, Springer Transactions on High-Performance Embedded Architectures and Compilers, Elsevier Journal of Parallel and Distributed Computing, Elsevier Signal Processing, Springer Journal of Supercomputing, Elsevier Journal of Systems Architecture, Elsevier The Journal of Systems and Software, Springer The Journal of Signal Processing Systems, Elsevier Journal of Real-Time Image Processing, Elsevier Integration, the VLSI Journal, Elsevier Computers and Mathematics with Applications, John Wiley & Sons International Journal of Circuit Theory and Applications.
- Review of textbooks for the IST Press (Academic Publisher, IST).

7.6 Professional Admissions and Promotions

12/2016 Member of the Committee to select and admit an Associate Professor for the Department of Electrical and Computer Engineering, Scientific Area of Electronics, IST, UL, Portugal.

01/2016 Member of the Committee to select and admit an Associate Professor for the Department of Electrical and Computer Engineering, Faculdade de Ciências e Tecnologia, Universidade de Coimbra, Portugal.

12/2014 Member of the Committee to select and admit a Full Professor for the Department of Computer Science and Computer Engineering, Scientific Area of Computer Architecture and Operating Systems, IST, UL, Portugal.

12/2014 Member of the Committee to select and admit an Assistant Professor for the Department of Electrical and Computer Engineering, Scientific Area of Computer Architecture, IST, UL, Portugal.

12/2013 Member of the Committee to select and admit an Associate Professor for the Department of Electrical and Computer Engineering, Scientific Area of Electronics, IST, UL, Portugal.

4/2013 External Advisor for a promotion to Associate Professor, University College Dublin, Ireland.

7.7 Reviewing/Referring of Theses

06/09/2016 Jury of the Ph.D. dissertation of Nuno Miguel Lourenço Diegues, "Algorithms for Enhancing the Performance Robustness of Transactional Memory Systems", at Department of Computer Science and Engineering, IST, UL, Portugal.

29/04/2016 Jury Member of the Ph.D. dissertation of Hamid Arabnejad, "QoS based workflow scheduling on heterogeneous resources", Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto, Portugal.

14/03/2016 Jury member of Dr. Octavian Adrian Postolache's Habilitation (Agregação in Portugal) at Department of Computer Science and Engineering, IST, UL, Portugal.

11/03/2016 Jury Member of the Ph.D. dissertation of Purnachand Nalluri, "A Fast Motion Estimation Algorithm and its VLSI Architecture for High Efficient Video Coding", Departamento de Eletrónica, Telecomunicações e Informática, Universidade de Aveiro, Portugal.

29/02/2016 Jury Member of the Qualifier Exam for the PhD of Roberto de Matos,"Unidade Aritmética Completa baseada em RNS para Alplicações com Ampla Faixa Dinâmica", Universidade Federal de Santa Catarina, Florianópolis, Brasil.

12/02/2016 Head of the Jury of the Ph.D. dissertation of Valter António Louzeiro Sádio, "Optimization of Charge Pump DC-DC Converters for Mobile Applications", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

29/01/2016 Jury Member of the Ph.D. dissertation of Sergio Santander Jiménez,"Multiobjective Analysis and Inference of Phylogenetic Hypotheses by Means of Parallel and Bioinspired Computing", Universidade de Extremadura (opponent), Spain.

26/01/2016 Jury Member of the Ph.D. dissertation of João Maria Duarte Andrade, "Design Space Exploration of LDPC Decoders on Programmable and Reconfigurable Architectures", at Department of Electrical and Computer Engineering, Universidade de Coimbra (opponent), Portugal.

23/10/2015 Jury Member of the Ph.D. dissertation of Rui Jorge Melo Teixeira, "Camera Calibration and Real-Time Image Processing in Heterogeneous Architectures – Application in Medical Endoscopy", at Department of Electrical and Computer Engineering, Universidade de Coimbra (opponent), Portugal.

09/10/2015 Jury Member of the Ph.D. dissertation of Rui Jorge Melo Teixeira, "Combining Predictive and Distributed Video Coding", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

14/09/2015 Jury of the Habilitation (Agregação in Portugal) of Dr. João Manuel Paiva Cardoso at Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto, Portugal.

23/07/2015 Head of the Jury of the Habilitation (Agregação in Portugal) of Dr. Pedro Manuel Santos de Carvalho at Department of Electrical and Computer Engineering, IST, UL, Portugal.

19/06/2015 Jury Member of the Ph.D. dissertation of Unai Lopez Novoa, "Contributions to the Efficient Use of General Purpose Coprocessors: Kernel Density Estimation as a Case Study", Universidad del País Vasco(opponent), Spain.

29/12/2014 Head of the Jury of the Ph.D. dissertation of Luís Filipe Soldado Granadeiro Rosado, "New Eddy Current Probes and Digital Signal Processing Algorithms for Friction Stir Welding Testing", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

29/12/2014 Head of the Jury of the Ph.D. dissertation of Tiago Miguel Lopes Marta da Costa, "Integrated Circuits for Interfacing Magnetoresistive Sensors: Applications to Biomedical Analysis and Eddy Current Testing", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

12/12/2014 Head of the Jury of the Ph.D. dissertation of Carlos João Oliveira Moreira, "Digital Control in Integrated DC-DC Converters", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

05/12/2014 Jury Member of the Ph.D. dissertation of Jorge Sevilla Cedillo, "A New Digital Repository for Hyperspectral Images based on Spectral Unmixing and Implemented on GPUs", Universidade de Extremadura (opponent), Spain.

04/12/2014 Head of the Jury of the Ph.D. dissertation of José Fernando de Jesus da Rocha, "Limitação da Tensão nos Dispositivos de Conversores CC-CC Integrados", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

17/11/2014 Head of the Jury of the Ph.D. dissertation of Nuno Miguel da Luz Neves Guerreiro, "Fault list compression for cost-effective analog and mixed-signal fault simulation", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

24/09/2014 Head of the Jury of the Ph.D. dissertation of Victor Manuel Antunes da Silva, "Reconfigurable Hardware using Magnetic Tunneling Junction Memories", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

19/09/2014 Head of the Jury of the Ph.D. dissertation of Maria Luísa Pedro Brito da Torre Caeiro, "Common Radio Resource Management in Virtual Heterogeneous Networks", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

08/09/2014 Head of the Jury of the Habilitation (Agregação in Portugal) of Dr. Nuno Horta at Department of Electrical and Computer Engineering, IST, UL, Portugal.

23/05/2014 Head of the Jury of the Ph.D. dissertation of Nuno Nogueira Dias, "High-Efficiency in Multi-Mode Integrated DC-DC Conversion", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

31/03/2014 Head of the Jury of the Habilitation (Agregação in Portugal) of Dr. Horácio Neto at Department of Electrical and Computer Engineering, IST, UL, Portugal.

26/02/2014 Head of the Jury of the Ph.D. dissertation of António Couto Pinto, "A Flash ADC Architecture Tolerant to High Offset Voltage Comparators", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

18/12/2013 Head of the Jury of the Ph.D. dissertation of Eduardo Pinheiro, "Unobstructive Vital Signs Monitoring of Wheelchair Users", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

1/9/2013 Examiner of the Ph.D. dissertation of Jeremy Low Yung Shern, "VLSI Efficient RNS Scalers and Arbitrary Modulus Residue Generators", Nanyang Technological University, Singapore.

16/9/2013 Jury Member of the Ph.D. dissertation of Nelson Silva, "Reconfigurable Transmitters for Software Defined Radio", Universidade de Aveiro (opponent), Portugal.

13/12/2012 Jury member at Dr. José Monteiro's Habilitation (Agregação in Portugal) at Department of Computer Science and Engineering, IST, UL, Portugal.

1/4/2012 Examiner of the Ph.D. dissertation of Ramya Muralidharan, "Novel modulo multipliers for moduli $2^n - 1, 2^n, 2^n + 1$", Nanyang Technological University, Singapore.

6/6/2011 Jury Member of the Ph.D. dissertation of Arnaldo Azevedo, "Efficient Execution of Video Applications on Heterogeneous Multi- and Many-Core Processors", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

21/12/2010 Jury Member of the Ph.D. dissertation of Kazeem Gbolagade, "Effective Reverse Conversion in Residue Number System Processors", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

15/11/2010 Jury Member of the Ph.D. dissertation of João Ascenço, "Distributed Video Coding: Improving the RD Performance", Department of Electrical and Computer Engineering, IST, UL (opponent), Portugal.

2/07/2010 Jury Member of the Ph.D. dissertation of José Caeiro, "Detecção e Agrupamento de Contornos"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

26/2/2010 Reviewer of the Ph.D. dissertaion of Otoniel Granado, "Fast and Efficient Coding Tools for Digital Image and Video Signals", *Departamento de Física Y Arquitectura de Computadores*, Universidad Miguel Hernández, Spain.

13/10/2008 Jury Member of the Ph.D. dissertation of Filipa Duarte, "A Cache-based Hardware Accelerator for Memory Data Movements", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

15/09/2008 Jury Member of the Ph.D. dissertation of Sandra Jardim, "Algoritmos para Representação Esparsa e Robusta de Sinais"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

29/8/2008 Jury Member of the Ph.D. dissertation of Daniel Larkin, "Energy Efficient Hardware Acceleration of Semantic Video Object Processing on Mobile Computing Platforms", School of Electronic Engineering, Dublin City University (opponent), Ireland.

18/7/2007 Jury Member of the Ph.D. dissertation of Paulo Nunes, "Rate Control for Object-based Video coding", Department of Electrical and Computer Engineering, IST, UL (opponent), Portugal.

8/6/2007 Jury Member of the Ph.D. dissertation of Arnaldo Oliveira, "Especialização e Síntese de Processadores para Aplicação em Sistemas de Tempo-Real"(thesis written in portuguese), Informatics, Telecommunications, and Electronics Department, Universidade de Aveiro (opponent), Portugal.

15/5/2006 Jury Member of the Ph.D. dissertation of Jaime Cardoso, "Metadata Assisted Image Segmentation", Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto (opponent), Portugal.

19/11/2004 Jury Member of the Ph.D. dissertation of Pyrrhos Stathis, "Sparse Matrix Vector Processing Formats", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

7/6/2004 Jury Member of the equivalence of the Ph. D. of José Rogado, "Aspects Materiels et Logiciels de la conception d'un systeme micro-ordinateur 16 bits", Department of Computer Science and Engineering, IST, UL, Portugal.

25/11/2002 Jury Member of the Ph.D. dissertation of Ana Freitas, "Estimação da Potência em Circuitos Digitais utilizando Técnicas de Enumeração Implícita"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

2/4/2001 Jury Member of the Ph.D. dissertation of João Paiva Cardoso, "Compilação de Algoritmos em Java para Sistemas Computacionais Reconfiguráveis com Exploração de Paralelismo ao Nível das

Operações"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

12/1/2001 Jury Member of the Ph.D. dissertation of Jorge Barbosa, "Paralelismo em Processamento e Análise de Imagens Médicas (thesis written in portuguese), Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto (opponent), Portugal.

15/10/1997 Jury Member of the Ph.D. dissertation of José Neto Fernandes, "A Interpretação de Imagens Texturadas"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

7.8 Reviewing of Grant Proposals and Projects

2016 Member of the evaluation panel in the area of ICT for the call for project proposals targeting 'Forcing Ahead with Research' from the Academy of Finland.

2014-16 Head of the National Panel for the final scientific evaluation of all projects in the area of Electrical Engineering funded by the FCT.

2014-16 Member of the National Panel for the scientific evaluation of the execution of the strategic plans of the research institutions for the year of 2014 funded by the FCT, in the areas of Computer Science and Electrical Engineering.

2015 Evaluator of Research Project Proposals to the H2020 program from the European Commission.

2015 Evaluator of Proposals of Projects under Scientific Bilateral Cooperation Agreements supported by FCT, namely within the scope of the FCT/CAPES (Brasil) Agreement.

2013 Evaluator of Applications to the "The Investigator Programme"of the Portuguese National Foundation for Science and Technology (FCT), which will contract 150 researchers at national level in three categories: Starting, Development and Consolidation of the research career.

2012 Member of the National Evaluation Panel for Fellowships and Grants in Computers Science and Electrical Engineering, Portuguese National Foundation for Science and Technology.

2012 Review of research grant proposals for the European Commission, EU Objective *ICT-2011.9.1: FET-Open - Challenging current Thinking* (FP7).

2012 Review of research grant proposals for the eScience Open Call for Converging Sciences, NWO, Netherlands.

2012 Review of research grant proposals for the Czech Science Foundation, the main public funding agency in the Czech Republic supporting all areas of basic scientific research.

2012 Review of research grant proposals for the Research Grants Council (RGC) of Hong Kong.

2011 Review of research grant proposals for the Research Grants Council (RGC) of Hong Kong.

2010 Review of research grant proposals for *Associate Teams program*, *l'Institut National de Recherche en Informatique et en Automatique* (INRIA), Paris, France.

2009 Review of research grant proposals for the *Earlier Carrer Research Excellence Award*, University of Auckland, New Zealand.

2008 Review of research grant proposals for the *Earlier Carrer Research Excellence Award*, University of Auckland, New Zealand.

2007 Review of research grant proposals for the European Commission, EU program *Information and Communication Technologies - Future & Emerging Technologies* (FP7-ICT-2007-C) (FP7).

2007 Review of research grant proposals for Programa Operacional Ciência e Inovação 2010, medida V.5 "Investigação, desenvolvimento tecnológico e inovação em cooperação europeia e internacional", Portuguese Foundation for Science and Technology (FCT).

2005 Review of research grant proposals for *Associate Teams program*, *l'Institut National de Recherche en Informatique et en Automatique* (INRA), Paris, France.

2004 Review of research grant proposals for the 2nd edition of the I&D Program of the Electrical and Computer Engineering Department of the Faculty of Engineering, University of Porto, Portugal.

7.9 Juries for awards

2016 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2015 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2015 Member of the jury for awarding the best PhD thesis at IST in the years 2013-2014 in the areas of Electrical Engineering, Commputer Science, Physics and Mathematics, "Abreu Faro Prize".

2014 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2013 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2012 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

7.10 Institutional Services

2016-2018 Member of the of the NATO Science for Peace and Security (SPS) Programme's 'Independent Scientific Evaluation Group' (ISEG).

2014-2016 Coordinator of the Committee for evaluating the scientific execution and outcome of all the research projects in the area of Electrical Engineering funded by the Portuguese Foundation for Science and Technology (FCT).

2013-2016 Member of the Scientific Council for the Exact Sciences and Engineering, composed by only 14 members chosen at National level, of the Portuguese Foundation for Science and Technology (FCT).

2012- Chair of the Commission D, in Electronics and Photonics, of the URSI-Portugal.

2009-2013 Chair of INESC-ID, a not for profit, privately owned institution of public interest, dedicated to advanced research and development in the domains of electronics, telecommunications and information technologies, with more than 1000 PhD researchers and owned by IST.

2015-2020 Member of Research Core Team and Management Committee of the Advanced Integrated Microsystems PhD Program, funded by the the Portuguese Foundation for Science and Technology (FCT) with a set of scholarships for 4 consecutive years.

2012-214 Member of the Scientific Council of the Doctoral Program in Electrical and Computer Engineering (PDEEC) at IST.

2002-2004 Member of the Scientific Committee of the Master in Electrical and Computer Engineering, responsible for the specialization in Electronics, IST.

2008-2012 Coordinator of the MSc and BSc programs in ECE at IST, with more than 1500 students.

2008-2012 Member of the Coordinating Committee of Pedagogical Council of IST.

2010-2012 Member of the Commission's strategy of the Department of Electrical and Computer Enginering, IST.

2004-2008 Member of the Board of Directors of INESC-ID.

2012-2016 Vice-President of the Scientific Council of IST, with responsibility for research and doctoral programs.

2009-2012 One of the 20 members of the Scientific Council of IST, that play an important role in the governance of IST

2006-2007 Member of the Scientific Council of IST, that play an important role in the governance of IST

2013-2016 Chair of the Executive Board of the Electronics' Scientific Area in the Electrical and Computer Engineering Department, IST.

2001-2003 Member of the Executive Board of the Electronics' Scientific Area in the Electrical and Computer Engineering Department, IST.

8 International Talks and Tutorials

02/10/2016 "Performance, Power and Energy-Efficiency Insightful Modeling of Multi-Cores", tutorial on The 34th IEEE International Conference on Computer Design Computer Architecture (ICCD), Phoenix, USA.

27/09/2016 "CARM: Cache-aware Roofline model for Multicores", Computer Architecture Lab at Carnegie Mellon, Pittsburgh, USA.

15/07/2016 "Balancing Performance, Power and Energy-Efficiency on Multi-cores towards Exascale Computing", University of Tokyo, Japan.

29/06/2016 "Cache-aware Modeling of Multi-cores: Performance, Power and Energy-Efficiency", invited talk, School of Computer Science and Systems Engineering at Kyushu Institute of Technology, Fukuoka, Japan.

25/05/2016 "Towards Asymmetric Post-Quantum Embedded Encryption", Invited Talk, Emerging Technologies: Communications, Microsystems, Optoelectronics, Sensors, Montreal, Canada.

12/04/2016 "Heterogeneous Systems for Multimedia and Cryptography", Distinguished Lecture Series, Singapore University of Technology and Design (SUTD), Singapore.

3/04/2016 "Application-aware Task Management for Emerging Embedding Systems", invited lecture in **Universidade Federal de Santa Catarina** (CTC-UFSC), IEEE Technical Chapter IM09/CAS04/COM19, Florianopolis, Brasil.

29/02/2016 "Cache-Aware Roofline Model: Performance, Power and Energy-Efficiency", 3 hours Tutorial on the VII IEEE Latin American Symposium on Circuits and Systems (LASCAS 2016), Florianopolis, Brasil.

23/11/2015 "CARM: Cache-Aware Performance, Power and Energy-Efficiency Roofline Modeling", in **Compiler, Architecture and Tools Conference** (CATC), Intel, Haifa, Israel.

30/10/2015 "Application Guided Task Management on Heterogeneous Embedded Systems", in **Workshop on Intelligent Solutions in Embedded Systems** (WISES), Invited Presentation, Ancona, Italy.

9/7/2015 "Energy-aware Task Management for Heterogeneous Low-Power Systems", in **Algorithms and Scheduling Techniques to Manage Resilience and Power Consumption in Distributed Systems**, Dagstuhl Seminar 15281, Germany.

26/9/2014 "Public-Key Cryptography on SIMD Embedded Engines", invited talk in the Centro de Investigación en Tecnoloxías da Información (CITIUS) Universidade de Santiago de Compostela. Spain.

1/7/2014 "Coping with Complexity: CPUs, GPUs and Real-world Applications", invited talk in the 9th *Scheduling in Aussois Workshop*, CNRS/INRIA, Lyon, France.

9/6/2014 "Modeling and Load Balancing for Multicore Systems", invited talk in the Department of Electrical and Computer Engineering (ECE), University of Auckland, New Zealand.

10/2/2014 "Overhauling Multicores Performance: Modeling and Load Balancing", keynote speaker in the 12th International Conference on Parallel and Distributed Computing and Networks, Innsbruck, Austria.

10/9/2013 "Monitoring Performance and Power for Application Characterization with Cache-aware Roofline Model", keynote speaker in the 10th International Conference on Parallel Processing and Applied Mathematics (PPAM), Warsaw, Poland.

26/6/2013 Organizes and chairs the breakout session on "Future Computing", integrated in the "*FET-Flagship HBP: Workshop on Human Brain Project: A roadmap for Portugal".*

24/5/2013 "Stream-based computing: Principles and case studies", invited talk in the Universidad Caceres, Spain.

6/2/2013 "Stream-based computing and fine-grained parallelism", invited talk in the Graduate School of Systems and Information Engineering, University of Tsukuba, Japan.

24/6/2011 "Distributed Computing on Highly Heterogeneous Systems", invited talk in the International Advanced Workshop on High Performance Computing, GRIDS and clouds (HPC 2011), Cetraro, Italy.

30/5/2011 *"Bandwidth-Aware Scheduling for On-Chip Cluster Architectures", invited talk in the 4th Scheduling in Aussois Workshop, CNRS/INRIA, Aussois, France.*

1/11/2010 *"RNS: Fundamentals and Applications", invited talk, Faculty of Electronic Engineering, University of Niš, Serbia.*

24/6/2010 *"Efficient Execution on Heterogeneous Systems", invited talk in the International Advanced Workshop on High Performance Computing, GRIDS and clouds (HPC 2010), Cetraro, Italy.*

2/6/2010 *"Cooperative Execution on Heterogeneous Multicore Systems", invited talk in the 3rd Scheduling in Aussois Workshop, CNRS/INRIA, Aussois, France.*

4/2/2010 *"Foreseeing the Role of Reconfiguration in Multicore Architectures", keynote speaker in the VI Jornadas sobre Sistemas Reconfiguráveis (REC'2010), Universidade de Aveiro, Portugal.*

16/12/2009 *"AES and EC Cryptographic Processor with Runtime Configuration", invited talk in the 17th International Conference on Advanced Computing and Communication, Bangalore, India.*

26/8/2009 *"Extending the application of GPUs beyond processing accelerators", Computer Engineering Colloquium, TU Delft, Netherlands.*

29/1/2009 *"Customizable Elliptic Curve Cryptography for Reconfigurable Devices", talk in the HiPEAC Reconfigurable Computing Cluster meeting, Paphos, Cyprus.*

20/11/2008 *"C(G)PUs: Arquitectura e Programação de Processadores Multicore", keynote speaker in the Quartas Jornadas de Engenharia de Electrónica e Telecomunicações e de Computadores, ISEL, Lisboa, Portugal.*

14/11/2008 *"Any-Core Memory-Centric Architecture for Advanced Video Coding", invited talk, Departamento Electrónica e Computación of Universidade de Santiago de Compostela, Spain.*

11/6/2008 *"What is so special in the Tomasulo hardware algorithm?", Seminar in the Seminal Seminar series, IST TagusPark, Portugal.*

26/8/2008 *"Stream-based concurrent computational models and programming tools", Invited talk in the Parallel Routines Optimization and Applications, Universidad de Murcia, Ministerio de Educación y Ciencia, Murcia, Spain.*

17/4/2007 *"Caravela: A Distributed Stream-Based Computing Platform", talk in the Compiler and Architecture Seminar, IBM Research Lab in Haifa, Israel.*

2/3/2007 *"Caravela distributed computing using stream-based processing", invited talk, Faculdade de Engenharia da Universidade do Porto, organizada em conjunto com o Instituto de Engenharia Biomédica.*

1/10/2003 *"Sistema de Visão Artificial não Invasivo", invited talk in the 2º Encontro de Engenharia Biomédica, Faculdade de Medicina da Universidade de Lisboa and IST, Portugal.*

9 Awarded Research Grants

9.1 Research funding

The first name corresponds to the Principal Investigator (PI).

2013-2016 Leonel Sousa (Member of the *Management Committee, Leader of Working Group 1 on "State of the art and continuous learning in Ultra Scale Computing Systems*), *et al.*, *Network for Sustainable Ultrascale Computing* (NESUS), EU ICT COST Action I1305.

2013-2016 Leonel Sousa, *Stretching the Limits of Parallel Processing on Heterogenous Computing Systems* (P2HCS), research project funded by the Portuguese Foundation for Science and Technology (FCT) (PTDC/EEI-ELC/3152/2012)- 153k €.

2012-2014 Leonel Sousa, NVIDIA CUDA Research Center INESC-ID/IST, one of 70 NVIDIA partners around the world - hardware and software donations and direct technology support.

2012- Leonel Sousa, Maxeler University Program INESC-ID/IST, - hardware and software donations, direct technology support, internships for students and collaborative research.

2011-2013 Nuno Roma, Leonel Sousa, *Heterogeneous Multicore Architecture for Biological Sequence Analysis* (HELIX), research project funded by the Portuguese Foundation for Science and Technology (FCT) (PTDC/EEA-ELC/ 113999/2009)- 200k €.

20011-2013 Sara Madeira, Leonel Sousa, *Understanding NEUROdegenerative diseases through CLINical and OMICS data integration* (NEUROCLINOMICS), research project funded by the FCT (PTDC/EEA-ELC/ 113999/2009)- 150k€.

2004-2015 Member of the *European Network of Excellence on High-Performance and Embedded Architecture and Compilation* (HiPEAC), FP7 - Information Society Technologies.

2010-2012 Ivan Milentijevic, Leonel Sousa, *et al.*, (PI, at national level) *National Platform for Knowledge Triangle in Serbia* (KNOWTS), Tempus Project, TEMPUS European (EU) Project (158881-TEMPUS-1-2009-1-RS-TEMPUS-JPHES).

2008-2013 Emmanuel Jeannot, Leonel Sousa (PI, at national level), *et al.*, *Open European Network for High Performance Computing on Complex Environments*, EU ICT COST Action IC0805.

2009-2010 Leonel Sousa, Jean-Claude Bajard, *Cryptographic Sistems based on Modular Arithmetic* (SCry-BAM), Research Program between Portugal and France- 6k€.

2009-2012 Harry Thewissen, Leonel Sousa, *et al.*, *Nanoelectronics for Safe, Fuel Efficient and Environment Friendly Automotive Solutions* (SE2A), EU *ENIAC Joint Undertaking.*

2008-2010 Moisés Piedade, Leonel Sousa, *Intracortical Neuronal Stimulator* (ICONS), research project funded by the FC)- 150k€.

2007-2009 João Lemos, Leonel Sousa, *Integrated Design for Automation of Anaesthesia* (IDEA), research project funded by the FCT (PTDC/EEA-ACR/69288/2006)- 100k€.

2005-2007 Leonel Sousa, *Adaptive H.264/AVC Motion Estimation Processor for Mobile and Battery Supplied Devices* (AMEP), research project funded by the FCT (FCT POSI/EEA-CPS/60765/2004)- 100k€.

2005-2008 Leonel Sousa, *Retina Neural Code: Accurate Modelling towards an Artificial Visual System* (RNC), research project funded by the FCT (FCT POSI/EEA-CPS/61779/2004)- 70k€.

2005-2006 Paulo Freitas, Leonel Sousa, *Magnetoresistive Biochip Microarray Platform for Biomolecular Recognition* (Biochip), research project funded by the FCT (FCT POSI/EEA-ESE/58523/2004)- 120k€.

2005 Leonel Sousa *Multimedia System for 3G Mobile Applications* (IVR), project funded by INOV - 10k€.

2002-2005 Eduardo Fernandez, Leonel Sousa, *al.*, *Cortical Visual Neuroprosthesis for the Blind* (CORTIVIS), EU project *key action 6* (QLK6-CT-2001-00279)- 200k€(budget for Portugal) .

2002-2004 Leonel Sousa, *Optimized and Reconfigurable Processing Structures for Motion Estimation* (COSME), research project funded by the FCT (FCT POSI/CHS/40877/2001) - 70k€.

1997-1999 *Developing Knowledge on ATM Technologies* (ATLANTIS), SINDEPEDIP, Medida 4.4, acção B 25/00167, Portuguese Ministry of Industry, responsible for the video coding component of the project - 40k€(800k PTE).

1990-1992 *Parallel Computing in Signal Processing and Environments for Concurrent Systems* (PARSEC-4121), EU "Parallel Computing Action"from the ESPRIT (ESPRIT PCA 4121).

9.2 Awards and Honors

2015 Selected ACM *Distinguished Scientist.*

2014 Designated Member of the *Design and Implementation of Signal Processing Systems Technical Committee* (DISP TC), IEEE Signal Processing Society.

2014 Designated Member of the IEEE *VLSI Systems & Applications Technical Committee* (VSATC), IEEE Circuits and Systems Society.

2013 Promoted to Fellow of the *Institution of Engineering and Technology* (IET), UK.

2010 Supervisor of the PhD thesis that got the second award of the 2010 **Fraunhofer Portugal Challenge**: "Flexible LDPC Decoders on Multicore Architectures", from Gabriel Falcão Fernandes (5k€).

2012-2010 Member of the Advisory Board of the *Computing Now*, from the IEEE Computer Society.

2009 **Best Researcher**, INESC -ID annual award to recognize the merit of their best researchers,the first edition of the award was exactly in 2009 (1k€). Jury of the prize: Prof. Srini Devadas (MIT), Prof. José Carlos Príncipe (University of Florida), Morris Sloman (Imperial College), and Franco Maloberti (University of Pavia).

2009, 2007 Two Honorable Mentions in the Scientific UTL/Santander Awards, which distinguish researchers or postdoctoral grantees from the Technical University of Lisbon that have published in the last five years in journals with more impact, based on the analysis provided by the ISI Web of Science.

2009 Supervisor of the MSc thesis awarded as the best MSc thesis in Instituto Superior Técnico in 2007/08 in the areas of Electrical and Computer Engineering and Informatics (award *Professor Luís Vidigal*, 5k€). Thesis "Portable Embedded Systems: Efficient Units for Data Processing and Cryptography", performed by Samuel Antão.

2009 Elevated to Senior Member of the *Association for Computing Machinery* (ACM).

2009 Designated member of the *International Federation for Information Processing* (IFIP), in the *Computer Systems Technology* Technical Committee (TC 10), *Concurrent Systems* Working Group (WG 10.3).

2004 Supervisor of the graduation thesis awarded as the best graduation thesis in Instituto Superior Técnico in 2002/2003 in the areas of Electrical and Computer Engineering and Informatics (award *Professor*

Luís Vidigal, 5k€). Thesis "Bio-Inspired Processing Module for the Development of an Artificial Retina", performed by Pedro Tomás.

2003 Elevated to Senior Member of the *Institute of Electrical and Electronics Engineers* (IEEE).

2003 Awarded with a scholarship from FCT, for a period of 6 months, to visit the *Delft University of Technology*, Delft, Holand.

1990 Awarded with a scholarship from NATO, for a period of 1 month, NATO Advanced Study Institute, University of Dundee, Scotland.

Best paper and poster awards:

2013 T. Dias, N. Roma, and L. Sousa, **Best Paper Award**, "High Performance Multi-Standard Architecture for DCT Computation in H.264/AVC High Profile and HEVC Codecs", Conference on Design and Architectures for Signal and Image Processing (DASIP2013),

2011 T. Dias, S. Lopez, N. Roma, and L. Sousa, "High Throughput and Scalable Architecture for Unified Transform Coding in Embedded H.264/AVC Video Coding Systems", **'Stamatis Vassiliadis' Best Paper Award**, 11th International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation (SAMOS XI), IEEE.

2010 T. Dias, N. Roma, and L. Sousa, **Best Poster Award**, "Hardware/Software Co-design of H.264/AVC Encoders for Multi-core Embedded Systems", Conference on Design and Architectures for Signal and Image Processing (DASIP2010),

2009 S. Antão, R. Chaves and L. Sousa, **HiPEAC Paper Award**, "Compact and Flexible Microcoded Elliptic Curve Processor for Reconfigurable Devices", The 17th Symposium on Field-Programmable Custom Computing Machines (FCCM), IEEE.